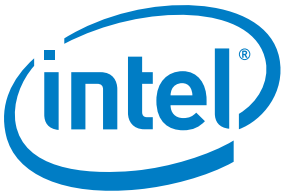

Intel® Quark™ microcontroller D1000

Datasheet

September 2015

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Revision History

Date	Revision	Description
July 2015	1.0	• Updated MCU Package and Pin-Out • Updated System Power Consumption Table
March 2015	0.6	Updated Section 4.5
January 2015	0.5	• Initial release

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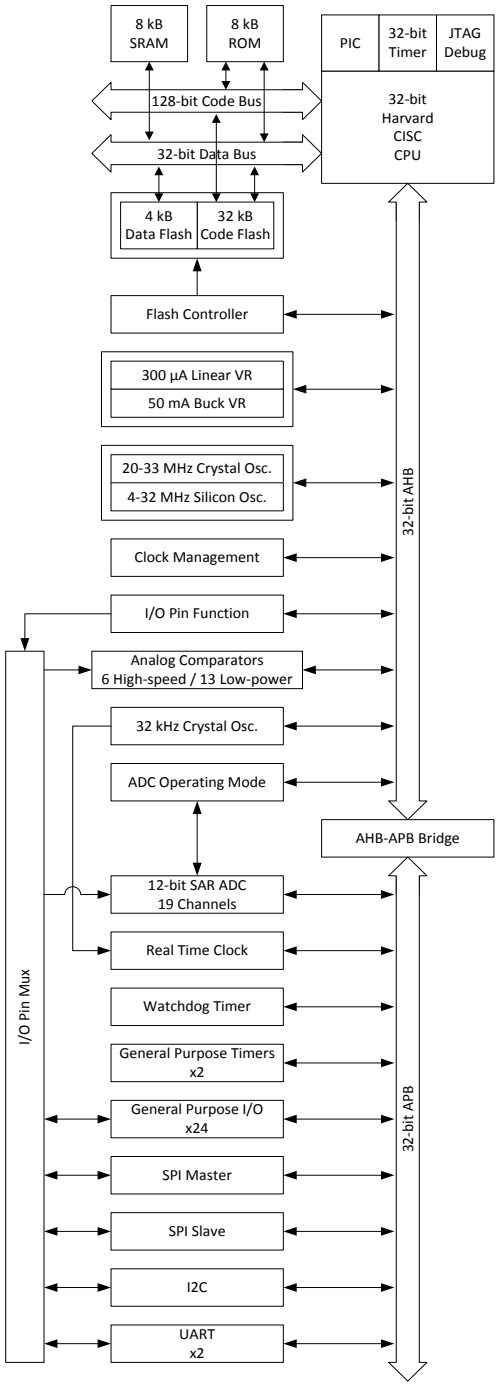
1.0 Introduction

The Intel® Quark™ microcontroller D1000 (MCU) is an extremely low power microcontroller at the top of its class in computational performance. It is optimized for long battery life applications such as wearable sensors and RFID tags. Its many features and benefits are presented in Figure 1.

Note: The Intel® Quark™ microcontroller D1000 is also called the MCU in this document.

Figure 1. Intel® Quark™ microcontroller D1000 Feature, Benefits and Block Diagram

- Powerful 32-bit Harvard CISC CPU with single cycle barrel shifter, two cycle multiplier, multi-cycle divider, integrated 32-bit timer, programmable interrupt controller, and JTAG debugger.
- 128-bit wide 32 kB code flash and 8 kB ROM with built in helper functions for CRC, AES, flash programming, self-calibration, and power management.
- 32-bit wide 8 kB SRAM and 4 kB data flash for system configuration and general purpose user non-volatile memory.
- 300 µA low quiescent current linear VR for low power sleep regimes and 50 mA buck VR for active regimes and off chip devices.
- 20-33 MHz crystal oscillator for low jitter precision frequency and 4-32 MHz silicon oscillator for reduced power.
- 32 kHz low power crystal oscillator and real-time clock for precise time keeping and wake up even during deep sleep regimes.
- Versatile fine grained clock management including branch gating and automatic fast frequency changes.
- Programmable analog, serial interface or GPIO functions on 24 pins.
- 19-channel 12-bit 2.4 MSps SAR ADC with 32-entry arbitrary channel scan table.
- Six high-speed and 13 low-power comparators for wake up, envelope detection, and demodulation functions.
- 32-bit watchdog timer with interrupt on first then reset on second expiration.
- Two 32-bit general purpose timers with independent clock frequencies.
- 24 general purpose I/O with edge detection and interrupt capability.
- Master and slave 16 Mbps serial peripheral interfaces supporting Motorola SPI, Texas Instruments SSP and National Semiconductor Microwire formats.
- I^2C master/slave interface supporting both 100 kbps standard and 400 kbps fast modes.
- Two UARTs with hardware handshaking.
- 24 ESD-protected versatile digital I/O buffers with high current drive and programmable direction, slew rate, and pull-up control.
- 19 ESD-protected analog inputs sharing the same pins as digital I/O for fast wake up from digital or analog input signals.
- Sleep regimes down to 1.5 µA.
- Wake up in as little as 2.0 µs.
- Active regimes down to 320 µA.
- Operating power supply range 1.62-3.63 V.



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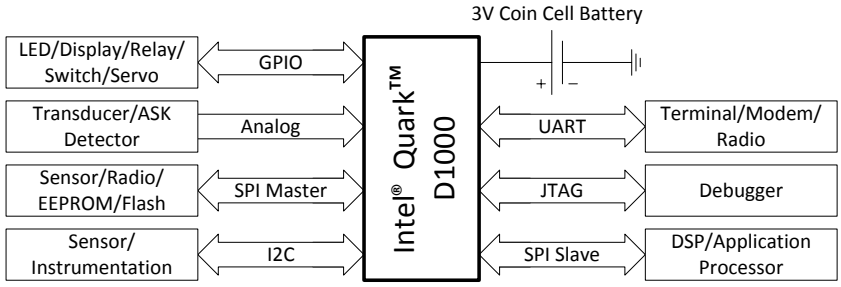
2.0 Applications and Usage

The Intel® Quark™ microcontroller D1000 supports a wide range of applications[1]. Its comparators and Analog-to-Digital Converters (ADC) make it easy to connect to transducers and RF front ends. Its serial peripheral interfaces make it easy to connect with popular sensors, radios, memories, DSPs and application processors. Its high drive current and slew rate controlled general purpose digital I/O with integrated pull-ups permit direct connection to LEDs, relays, and switches. The MCU's high performance CPU can support compute-intensive security and signal processing tasks beyond the reach of many of its peers. It can operate from a single 3.3 V battery with a discharge curve from 3.6 V down to 2.0 V and has comprehensive power management for extended battery life. Optionally, the MCU's integrated voltage regulator can be disabled and it can operate from a single regulated 1.8 V ± 10% power supply. All features and operating frequencies are available over the full input voltage range.

The Intel® Quark™ microcontroller D1000 has extremely versatile I/O capabilities. Package pins can be configured for analog, general purpose digital, or serial I/O. Unlike some of its peers, all of the MCU's serial interfaces can be used simultaneously. General purpose digital I/Os are bidirectional. When operating as outputs they can be open drain or push-pull with slew rate control. When operating as inputs they can be level sensitive, or edge detecting, with the ability to generate interrupts. An example application is shown in Figure 2.

Figure 2. Example Application Demonstrating Usage of All MCU Interfaces



Each analog input is connected to both an ADC channel and a comparator. The comparators have rail-to-rail common mode range with threshold supplied on a pin. Alternately, an internal 0.95 V threshold can be used. Since analog and digital inputs share common pins, comparators can wake the MCU up from both analog and digital signals.

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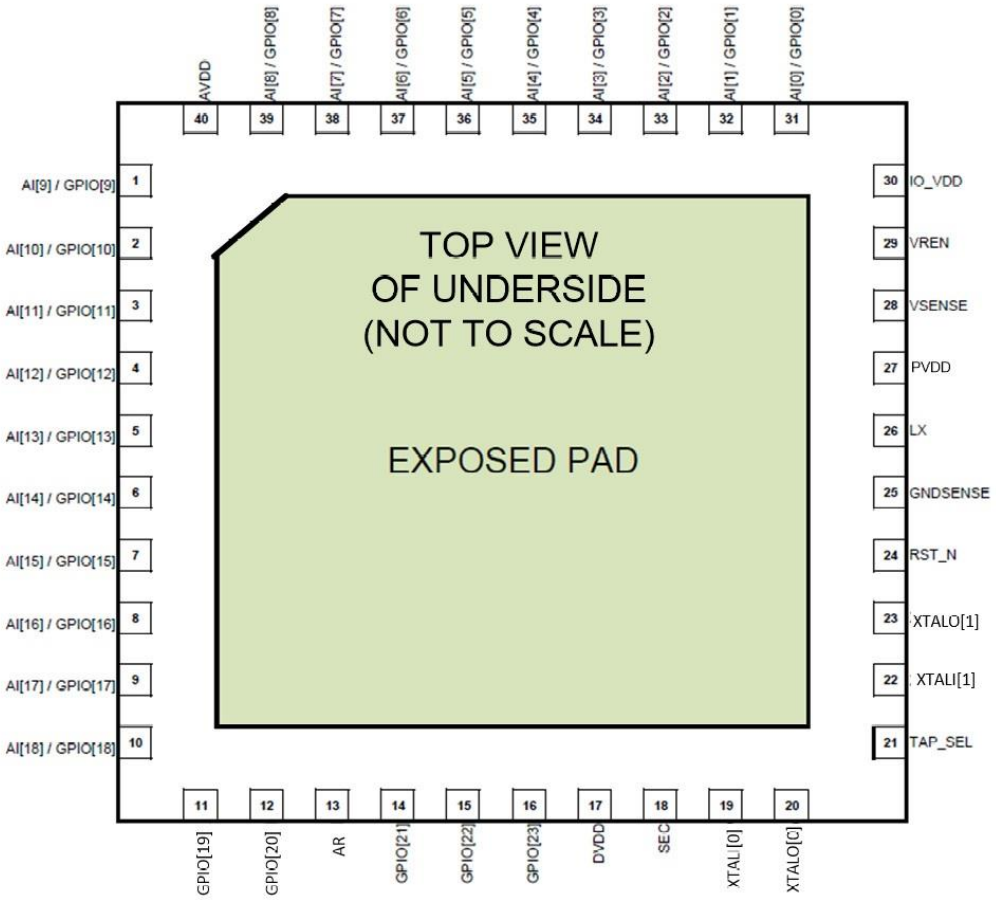
[1] Refer to the Intel® Quark™ microcontroller D1000 User Guide for details on memory map, register bit definitions, and helper functions.

3.0 Package and Pin-Out

The Intel® Quark™ microcontroller D1000 is packaged in a 6x6 mm 40 pin QFN. The package pin-out is shown in Figure 3.

Figure 3. MCU Package Pin-Out (Top View)



GPIO pin functions are multiplexed on the MCU. After power-on or reset, pin function defaults to code #3, where all GPIO pins are in a high impedance state and only analog functions are enabled. Software can select GPIO or serial communication pin functions by changing a single bit of the function code to zero. This avoids glitches that could result if both bits were to change at once.

Even though a digital pin function has been selected, analog functions on that pin are still possible. This permits wake-up using an analog comparator on a digital input. Table 1 lists the functions available on each pin. All pins have built-in ESD protection.

Table 1. MCU Pin Function By Function Code

Package Pin	Pin Function Code			
	#0	#1	#2	#3
1	AI[9]	GPIO[9]	SLV_M2SD	AI[9]
2	AI[10]	GPIO[10]	SLV_S2MD	AI[10]
3	AI[11]	GPIO[11]	SLV_M2SS	AI[11]
4	AI[12]	GPIO[12]	TXD[1]	AI[12]
5	AI[13]	GPIO[13]	RXD[1]	AI[13]
6	AI[14]	GPIO[14]	RTS[1]	AI[14]
7	AI[15]	GPIO[15]	CTS[1]	AI[15]
8	AI[16]	GPIO[16]	MST_M2SC	AI[16]
9	AI[17]	GPIO[17]	MST_M2SD	AI[17]
10	AI[18]	GPIO[18]	MST_S2MD	AI[18]
11	-	GPIO[19]	TDO	-
12	TXD[0]	GPIO[20]	TRST_N	-
13	AR	AR	AR	AR
14	RXD[0]	GPIO[21]	TCK	-
15	RTS[0]	GPIO[22]	TMS	-
16	CTS[0]	GPIO[23]	TDI	-
17	DVDD	DVDD	DVDD	DVDD
18	SEC	SEC	SEC	SEC
19	XTALI[0]	XTALI[0]	XTALI[0]	XTALI[0]
20	XTALO[0]	XTALO[0]	XTALO[0]	XTALO[0]
21	TAP_SEL	TAP_SEL	TAP_SEL	TAP_SEL
22	XTALI[1]	XTALI[1]	XTALI[1]	XTALI[1]
23	XTALO[1]	XTALO[1]	XTALO[1]	XTALO[1]
24	RST_N	RST_N	RST_N	RST_N
25	GSENSE	GSENSE	GSENSE	GSENSE
26	LX	LX	LX	LX
27	PVDD	PVDD	PVDD	PVDD
28	VSENSE	VSENSE	VSENSE	VSENSE
29	VREN	VREN	VREN	VREN
30	IOVDD	IOVDD	IOVDD	IOVDD
31	AI[0]	GPIO[0]	MST_M2SS[0]	AI[0]
32	AI[1]	GPIO[1]	MST_M2SS[1]	AI[1]

Package Pin	Pin Function Code			
	#0	#1	#2	#3
33	AI[2]	GPIO[2]	MST_M2SS[2]	AI[2]
34	AI[3]	GPIO[3]	MST_M2SS[3]	AI[3]
35	AI[4]	GPIO[4]	-	AI[4]
36	AI[5]	GPIO[5]	MST_S2M_SS	AI[5]
37	AI[6]	GPIO[6]	SCL	AI[6]
38	AI[7]	GPIO[7]	SDA	AI[7]
39	AI[8]	GPIO[8]	SLV_M2SC	AI[8]
40	AVDD	AVDD	AVDD	AVDD
Pad	VSS	VSS	VSS	VSS

JTAG pins are disabled by default. However, they will be enabled if flash is found to be erased or corrupted, if the system configuration stored in flash enables them, or if the user application enables them. This prevents exposure of any secrets the user may store in flash. The SEC pin can be used to securely force enablement of JTAG if the application developer is accidently locked out or returned units need failure analysis or reprogramming. The bootstrap procedure checks the SEC pin and erases flash (if configured to do so) then enables JTAG if a floating or logic high condition is found. SEC, along with a comparator, can be used for tamper detection as well.

Table 2 provides a detailed description of each pin function.

Table 2. Detailed Pin Function Description

Interface	Pin Name	Type	Description
Power	VSS	Ground	QFN package ground plane
	DVDD	Supply	1.35 – 1.8 V regulated core power supply.[1]
	PVDD	Supply	2.0-3.6 V unregulated VR power supply.[2,3]
	AVDD	Supply	1.6-3.6 V analog power supply[3]
	IOVDD	Supply	1.6-3.6 V I/O power supply[3]
	VSENSE	Analog input	Core power voltage sense
	GSENSE	Analog input	Core power ground sense
	LX	Supply	Core voltage regulator supply[4]
	VREN	Analog input	Voltage regulator enable: PVDD = enable VSS = disable
Clocking	XTALI[0]	Logic input	Crystal/oscillator input
	XTALO[0]	Logic output	Crystal output
	XTALI[1]	Logic input	Crystal/oscillator input

Interface	Pin Name	Type	Description
	XTALO[1]	Logic output	Crystal output
Reset	RST_N	Analog input	Low true reset with hysteresis. Tie to AVDD for internal power-on reset. <0.8 V = reset >1.1 V = not reset
	SEC	Logic input	Security
GPIO	GPIO[23:0]	Logic I/O	General purpose I/O
I^2C	SCL	Logic I/O	Open drain clock
	SDA	Logic I/O	Open drain data
UART	TXD[1:0]	Logic output	Transmit data
	RXD[1:0]	Logic input	Receive data
	RTS[1:0]	Logic output	Request to send
	CTS[1:0]	Logic input	Clear to send
Slave SPI	SLV_M2SC	Logic input	Clock
	SLV_M2SD	Logic input	Receive data (MOSI)
	SLV_M2SS	Logic input	Slave select
	SLV_S2MD	Logic output	Transmit data (MISO)
Master SPI	MST_M2SC	Logic output	Clock
	MST_M2SD	Logic output	Transmit data (MOSI)
	MST_M2SS[3:0]	Logic output	Slave select
	MST_S2MD	Logic input	Receive data (MISO)
	MST_S2MSS	Logic input	Slave select from other master(s)
Analog	AI[18:0]	Analog input	Comparator/ADC inputs
	AR	Analog input	Comparator reference
JTAG	TRST_N	Logic input	TAP controller reset
	TDI	Logic input	TAP data input
	TMS	Logic input	TAP mode select
	TCK	Logic input	TAP clock
	TDO	Logic output	TAP data output
	TAP_SEL	Logic input	TAP select 0 = Debug TAP 1 = Scan TAP

NOTES:

1. Digital I/O operation is degraded below 1.62 V and timing is not guaranteed.
2. Voltage range of PVDD is 1.6-3.6 V when the integrated VR is disabled.

Interface	Pin Name	Type	Description
3. AVDD, IOVDD and PVDD may be AC isolated, but must be supplied from a common power source. 4. A 47 µH and 4.7 µF external LC filter is required between LX and DVDD when the integrated VR is enabled.			

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4.0 Functional Description

The following section provides a detailed functional description of the Intel® Quark™ microcontroller D1000.

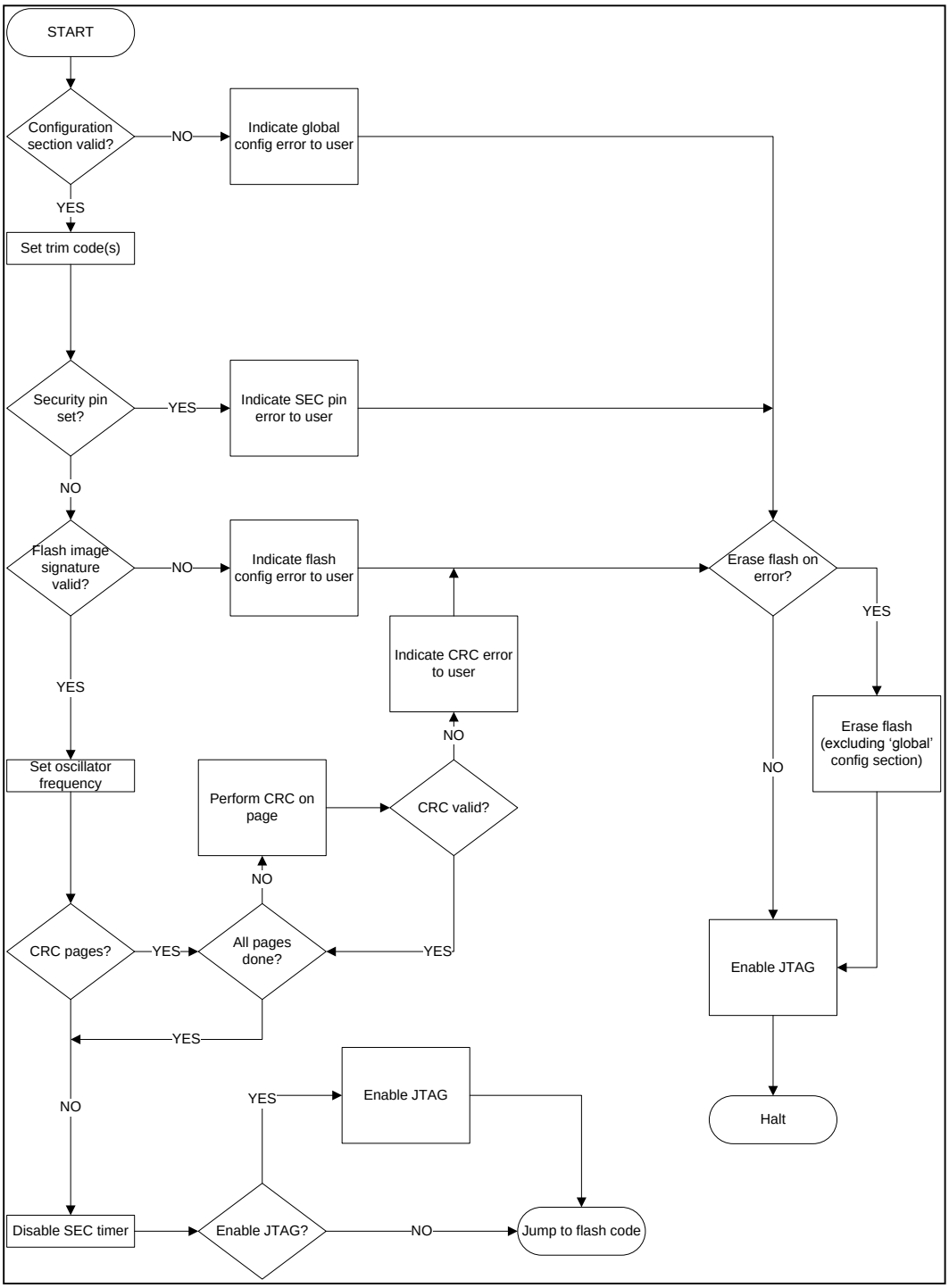
4.1 Power-on and Reset

The MCU has a built in power-on reset. In addition, the RST_N pin provides a user asserted low true reset. RST_N is an analog input with hysteresis that can be strapped to AVDD, connected to an RC delay pulled-up to DVDD to extend reset duration or driven by some external logic. If RST_N is less than 0.788 V, reset is active. If RST_N is greater than 1.112 V, reset is inactive. The actual threshold is somewhere in between with no less than 3.4 mV hysteresis.

While reset is active, all GPIO pins are in the high impedance state. A low to high transition on reset causes the MCU to reboot from integrated ROM. A configuration table is provided in the upper data page of flash memory to control the bootstrap process. Figure 4 shows a flowchart of the bootstrap procedure. The bootstrap procedure begins by checking for a valid configuration section in flash. This is indicated by a predefined signature stored at a fixed location. If the signature matches the predefined value, oscillator trim data and various configuration options stored in flash are processed. Any other signature value results in the processor halting with JTAG enabled and flash erased if so configured.

Oscillator trim data stored in the configuration section is applied to the silicon oscillator. This data is computed at the factory and can be recomputed by the user to calibrate to non-standard frequencies and operating conditions. Other configuration options include the presence of a valid program in flash and optional CRC checks. If there is a valid program in flash and the required CRC checks pass, the bootstrap program jumps to it. If there is no valid program in flash or a CRC check fails, the bootstrap program enables JTAG and halts with flash erased if so configured.

Figure 4. Bootstrap Flowchart Showing Security Checks and JTAG Enabling



One final configuration option is how to proceed in case of a bootstrap failure. For secure applications, the bootstrap procedure can be configured to erase flash just prior to JTAG enabling. For unsecure applications, JTAG is enabled without erasing flash, allowing the contents of flash to be examined for failure analysis. If the bootstrap procedure ends in processor halt, error information will be stored at addresses **0x6000 1000** and **0x6000 1004**. The format of error information is shown in Table 3.

Table 3. Bootstrap Error Codes

Error Type	Error Code in Address 0x6000 1000	Extended Information in address 0x6000 1004
ROM_CRC_ERROR	0x0000 0001	Starting address of page with error
ROM_INV_GLOBAL_SIG	0x0000 0002	-
ROM_INV_FLASH_SIG	0x0000 0003	-
ROM_SEC_SET	0x0000 0004	-

4.2 Clocking

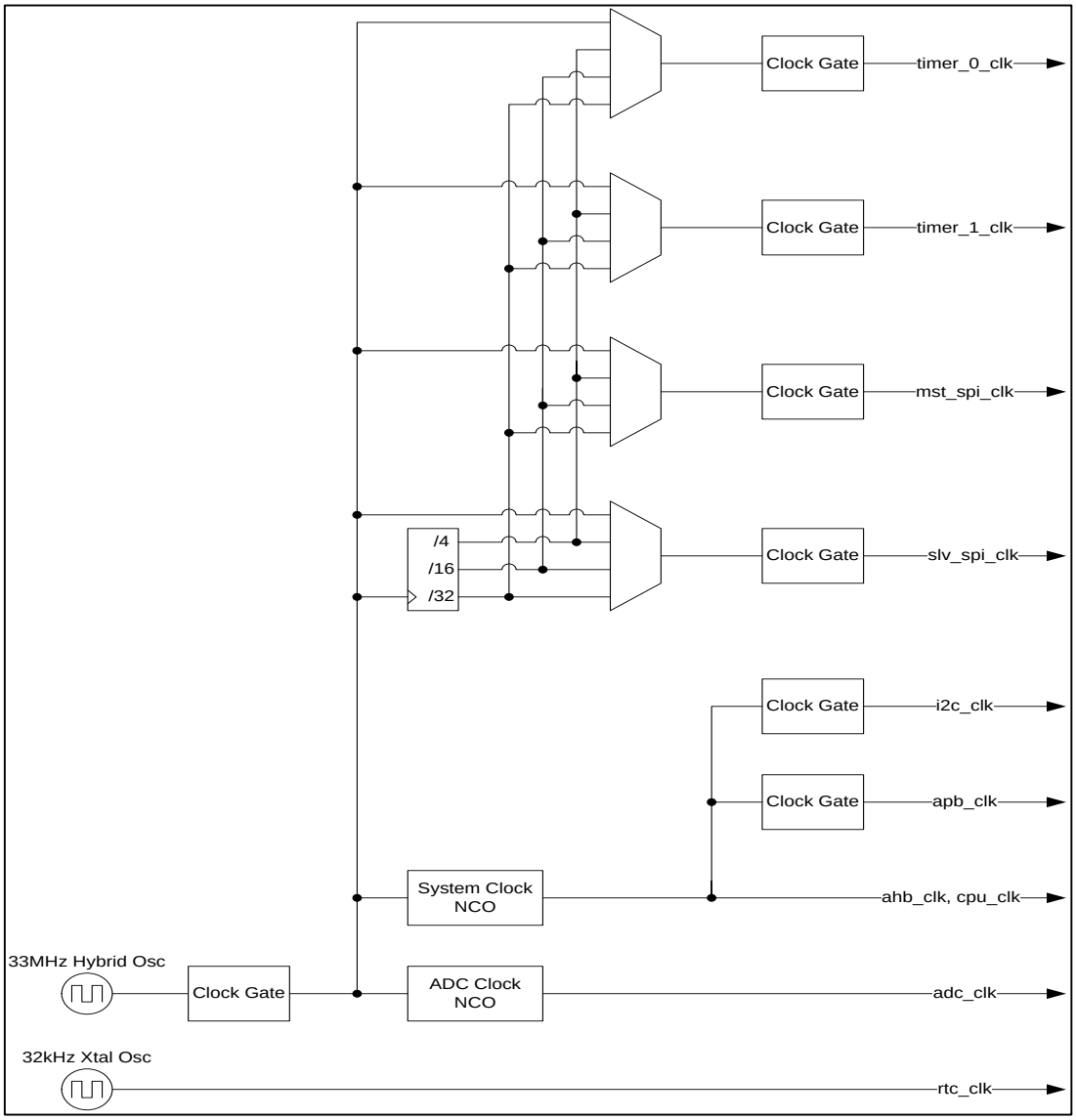
The MCU provides the user with fine-grained clock management. A schematic diagram of the clock network is shown in Figure 5. All clocks except the real-time clock are derived from the same oscillator. They are pseudo-synchronous, meaning that frequencies may differ, but edges align. While signals transferring between clock domains do not require resynchronization, a request-acknowledge handshake is used to ensure that signals are sampled.

The 33 MHz hybrid oscillator has a frequency range from 3.3-33 MHz and a shutdown mode for power savings. It provides the system clock source for the processor, the Advanced Microcontroller Bus Architecture* (AMBA) subsystem, and ADC. It is a hybrid silicon-crystal design providing a flexible clocking solution, which allows the user application program to trade off power consumption, settling time, jitter and frequency accuracy. Features include:

- Glitch-free switching from crystal to silicon oscillator modes and vice-versa.
- Low leakage shutdown mode with glitch-free power on.
- Fast start up and reduced power consumption in silicon oscillator mode.
- Fast switching 4, 8, 16 and 32 MHz frequency octaves in silicon oscillator mode.
- Low-jitter, high-precision frequency in crystal oscillator mode.
- Crystals in the range of 20-33 MHz are supported.
- External clock input using crystal pin XTALI[0].

In silicon oscillator mode, power is reduced at the expense of increased jitter and frequency error. The trim range for or the various frequency octaves is ±50% and the PVT variation of untrimmed frequency is around ±35%. Once trimmed, the Process-Voltage-Temperature (PVT) frequency variation is less than ±2% in the trimmed octave and less than ±4% in untrimmed octaves. The MCU is trimmed at the factory at 32 MHz. Crystals used with this oscillator must have maximum ESR of 50 ohms at 20 MHz and 80 ohms at 33 MHz. Suitable crystals include the ABM8G series by Abracon* (Abracon Corp., 2011).

Figure 5. Schematic Diagram of Clock Network Showing Branch NCOS, Dividers, and Gates



The 32 kHz crystal oscillator provides the clock source for the real-time clock. It also has a shutdown mode for power savings and external clock input using crystal pins. Suitable crystals include the ABS06 series by Abracon (Abracon Corp., 2011).

The system clock Numerically Controlled Oscillator (NCO) provides the clock source for the CPU, AHB, APB, watchdog timer, UART and I²C. In order to support applications requiring time synchronization with a remote time reference, the NCO provides fine frequency adjustments of 3.125%. The NCO supports the programmable divide ratios listed in Table 4 (negative frequencies indicate phase reversal). The default phase increment following reset is 0 (NCO bypass). Phase increments that are powers of two generate a jitter free output. Other phase increments result in clock jitter of no more than 3.125% of the crystal oscillator period. Changing the NCO phase increment affects a change in the NCO output frequency beginning with the next output clock edge. A change in phase increment can be immediate (on the next clock edge after writing) or in response to an event (for example, an interrupt).

Table 4. System Clock NCO Phase Increments and Corresponding Divide Ratios

Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio
1	0.03125	2	0.06250	3	0.09375	4	0.12500
5	0.15625	6	0.18750	7	0.21875	8	0.25000
9	0.28125	10	0.31250	11	0.34375	12	0.37500
13	0.40625	14	0.43750	15	0.46875	16	0.50000
17	-0.46875	18	-0.43750	19	-0.40625	20	-0.37500
21	-0.34375	22	-0.31250	23	-0.28125	24	-0.25000
25	-0.21875	26	-0.18750	27	-0.15625	28	-0.12500
29	-0.09375	30	-0.06250	31	-0.03125	0	1.00000

The ADC NCO generates integer frequency ratios of the input clock from 1:256 to 128:256 in 1:256 steps or undivided pass through. It too has a disable mode for power savings. An 8-bit phase accumulator permits fine frequency adjustments of 0.390625%. This NCO supports the divide ratios listed in Table 5 (negative frequencies indicate phase reversal and the default phase increment following reset is 1). At a crystal frequency of 32 MHz, the ADC clock frequency programming resolution would be 32 MHz / 256 = 125 kHz. A lower frequency crystal results in proportionally finer frequency resolution. When the ADC is disabled, the ADC clock is also disabled.

Table 5. ADC Clock NCO Phase Increments and Corresponding Divide Ratios

Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio
1	0.00390625	2	0.00781250	3	0.01171875	4	0.01562500
5	0.01953125	6	0.02343750	7	0.02734375	8	0.03125000
9	0.03515625	10	0.03906250	11	0.04296875	12	0.04687500

Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio
13	0.05078125	14	0.05468750	15	0.05859375	16	0.06250000
17	0.06640625	18	0.07031250	19	0.07421875	20	0.07812500
21	0.08203125	22	0.08593750	23	0.08984375	24	0.09375000
25	0.09765625	26	0.10156250	27	0.10546875	28	0.10937500
29	0.11328125	30	0.11718750	31	0.12109375	32	0.12500000
33	0.12890625	34	0.13281250	35	0.13671875	36	0.14062500
37	0.14453125	38	0.14843750	39	0.15234375	40	0.15625000
41	0.16015625	42	0.16406250	43	0.16796875	44	0.17187500
45	0.17578125	46	0.17968750	47	0.18359375	48	0.18750000
49	0.19140625	50	0.19531250	51	0.19921875	52	0.20312500
53	0.20703125	54	0.21093750	55	0.21484375	56	0.21875000
57	0.22265625	58	0.22656250	59	0.23046875	60	0.23437500
61	0.23828125	62	0.24218750	63	0.24609375	64	0.25000000
65	0.25390625	66	0.25781250	67	0.26171875	68	0.26562500
69	0.26953125	70	0.27343750	71	0.27734375	72	0.28125000
73	0.28515625	74	0.28906250	75	0.29296875	76	0.29687500
77	0.30078125	78	0.30468750	79	0.30859375	80	0.31250000
81	0.31640625	82	0.32031250	83	0.32421875	84	0.32812500
85	0.33203125	86	0.33593750	87	0.33984375	88	0.34375000
89	0.34765625	90	0.35156250	91	0.35546875	92	0.35937500
93	0.36328125	94	0.36718750	95	0.37109375	96	0.37500000
97	0.37890625	98	0.38281250	99	0.38671875	100	0.39062500
101	0.39453125	102	0.39843750	103	0.40234375	104	0.40625000
105	0.41015625	106	0.41406250	107	0.41796875	108	0.42187500
109	0.42578125	110	0.42968750	111	0.43359375	112	0.43750000
113	0.44140625	114	0.44531250	115	0.44921875	116	0.45312500
117	0.45703125	118	0.46093750	119	0.46484375	120	0.46875000
121	0.47265625	122	0.47656250	123	0.48046875	124	0.48437500
125	0.48828125	126	0.49218750	127	0.49609375	128	0.50000000
129	-0.49609375	130	-0.49218750	131	-0.48828125	132	-0.48437500
133	-0.48046875	134	-0.47656250	135	-0.47265625	136	-0.46875000
137	-0.46484375	138	-0.46093750	139	-0.45703125	140	-0.45312500
141	-0.44921875	142	-0.44531250	143	-0.44140625	144	-0.43750000
145	-0.43359375	146	-0.42968750	147	-0.42578125	148	-0.42187500

Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio	Φ Inc.	Div. Ratio
149	-0.41796875	150	-0.41406250	151	-0.41015625	152	-0.40625000
153	-0.40234375	154	-0.39843750	155	-0.39453125	156	-0.39062500
157	-0.38671875	158	-0.38281250	159	-0.37890625	160	-0.37500000
161	-0.37109375	162	-0.36718750	163	-0.36328125	164	-0.35937500
165	-0.35546875	166	-0.35156250	167	-0.34765625	168	-0.34375000
169	-0.33984375	170	-0.33593750	171	-0.33203125	172	-0.32812500
173	-0.32421875	174	-0.32031250	175	-0.31640625	176	-0.31250000
177	-0.30859375	178	-0.30468750	179	-0.30078125	180	-0.29687500
181	-0.29296875	182	-0.28906250	183	-0.28515625	184	-0.28125000
185	-0.27734375	186	-0.27343750	187	-0.26953125	188	-0.26562500
189	-0.26171875	190	-0.25781250	191	-0.25390625	192	-0.25000000
193	-0.24609375	194	-0.24218750	195	-0.23828125	196	-0.23437500
197	-0.23046875	198	-0.22656250	199	-0.22265625	200	-0.21875000
201	-0.21484375	202	-0.21093750	203	-0.20703125	204	-0.20312500
205	-0.19921875	206	-0.19531250	207	-0.19140625	208	-0.18750000
209	-0.18359375	210	-0.17968750	211	-0.17578125	212	-0.17187500
213	-0.16796875	214	-0.16406250	215	-0.16015625	216	-0.15625000
217	-0.15234375	218	-0.14843750	219	-0.14453125	220	-0.14062500
221	-0.13671875	222	-0.13281250	223	-0.12890625	224	-0.12500000
225	-0.12109375	226	-0.11718750	227	-0.11328125	228	-0.10937500
229	-0.10546875	230	-0.10156250	231	-0.09765625	232	-0.09375000
233	-0.08984375	234	-0.08593750	235	-0.08203125	236	-0.07812500
237	-0.07421875	238	-0.07031250	239	-0.06640625	240	-0.06250000
241	-0.05859375	242	-0.05468750	243	-0.05078125	244	-0.04687500
245	-0.04296875	246	-0.03906250	247	-0.03515625	248	-0.03125000
249	-0.02734375	250	-0.02343750	251	-0.01953125	252	-0.01562500
253	-0.01171875	254	-0.00781250	255	-0.00390625	0	1.00000000

The APB, I²C, CPU and AHB clocks (apb_clk, I²C_clk, cpu_clk and ahb_clk respectively), are at the same frequency. However, I²C and APB clock are gated. Four of the five peripheral clocks (timer_1_clk, timer_0_clk, slv_spi_clk, and mst_spi_clk) allow software to select between 1:1, 1:4, 1:16, or 1:32 integer frequency ratios of the AHB clock or gated off entirely. This allows the CPU clock frequency to be adjusted up or down depending on workload without affecting timers or SPI transactions. The clock mux and gate are glitch free.

Here are some important restrictions to note with respect to clock frequencies:

- `apb_clk` must be running for APB peripherals to generate interrupts
- $f_{SPI\_CLK} \leq f_{APB\_CLK}$
- $f_{SPI\_1\_CLK} \leq f_{APB\_CLK}$
- $f_{TIMER\_N\_CLK} \leq f_{APB\_CLK}$

4.3 Integrated Voltage Regulators (VR)

The MCU includes two integrated VRs:

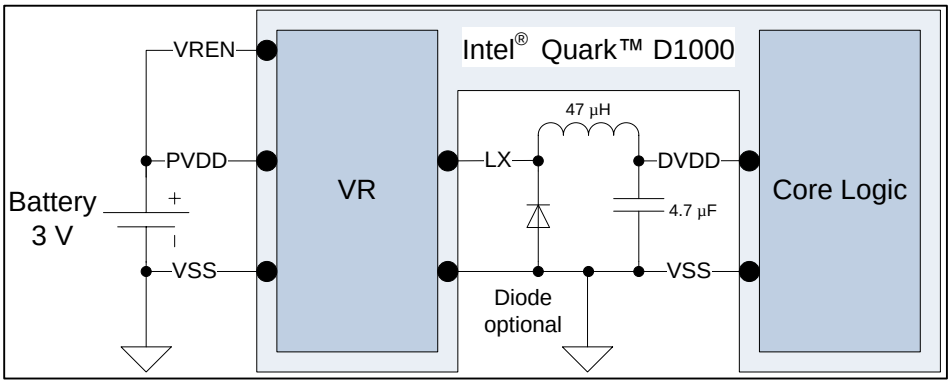
1. A 300 µA low quiescent current linear VR for low power sleep regimes.
2. A 50 mA buck VR for active regimes and powering external devices.

In addition to choosing the optimal regulator for the operating regime, the application program can also adjust the core voltage from 1.35 to 1.8 V. Lowering core voltage reduces leakage current, but care must be taken not to exceed the maximum clock frequency for that voltage.

For this reason a helper function has been provided in ROM to safely enter retention (i.e. reduced voltage) state. Also, the VR control/status register is password protected to prevent accidental misprogramming of the VR.

The buck regulator is capable of supplying much more current than the MCU can consume. The excess current can be used to power external devices. When powering external devices, they should be connected to the DVDD net and the sum of the MCU supply current plus the external device supply current must not exceed the 50 mA load current limit of the buck regulator. The buck regulator requires an external LC filter. Figure 6 shows how the LC filter should be connected to the package pins. Optionally, a Schottky diode with low reverse current and low forward voltage drop can be connected cathode to the LX pin and anode to VSS to improve VR efficiency.

Figure 6. Schematic Diagram Showing Connection of External Components to on Die VR



For applications where a regulated 1.8 V supply is available, the VR can be disabled entirely by strapping the VREN input to VSS. In this use case, AVDD, PVDD, IOVDD and DVDD should all be connected to the 1.8 V supply. Appropriate filtering should be used to provide AC isolation between them if noise contamination on AVDD is a concern.

4.4 Fine-Grained Power Management

The MCU provides fine-grained power management. Power consumption can be fine-tuned to the user application by powering down unneeded modules, shutting off unneeded clocks and adjusting the frequencies of others. However, in order to facilitate discussion of features and characterization we will broadly define five discrete power states:

- Active – In this state, the CPU is executing. All pipeline, memory, and AHB clocks are running. The core voltage is at 1.8 V and the buck regulator is selected.
- Halt – In this state, the CPU is halted. All pipeline, memory, and AHB clocks are stopped. The core voltage is at 1.8 V and the buck regulator is selected. Wake-up comes from any unmasked interrupt.
- ADC Sleep – In this state, all clocks except ADC (and optionally the 32 kHz oscillator) are stopped. The core voltage is set to 1.8 V and the buck regulator is selected. Wake-up comes from the ADC.
- Standby – In this state, all clocks are stopped (except optionally the 32 kHz oscillator). The core voltage is set to 1.8 V and the linear regulator is selected. Digital I/O may be enabled, but should not be switching. SEC must be de-asserted (strapped to VSS) so as not to cause wake up. Wake-up comes from the real-time clock or a comparator.
- Retention – In this state, all clocks are stopped (except optionally the 32 kHz oscillator). The core voltage is set to 1.35 V and the linear regulator is selected. Digital I/O may be enabled, but should not be switching. SEC must be de-asserted (strapped to VSS) so as not to cause wake-up. Wake-up comes from the real-time clock or a comparator.

4.4.1 Halt State

Halt state is entered whenever a halt instruction is executed. Exit from halt state occurs when an unmasked interrupt is received. After servicing the interrupt, execution continues with the instruction following the halt. This is typically used with interrupt driven programs that have an idle main loop. Resumption of active state is within 2 clocks of an interrupt event.

4.4.2 ADC Sleep State

ADC sleep state is entered by stopping all clocks except ADC clock (and optionally the 32 kHz oscillator) midstream. Exit from ADC sleep state occurs when the ADC completes a conversion operation. Interrupt service is optional since masking the ADC interrupt does not prevent wake-up. This is typically used in programs that can sleep (for example, all peripherals are stopped) and then periodically wake-up to process an ensemble of analog samples. Resumption of active state is typically within 2 µs of completion of the ADC conversion command (see 4.17 Analog to Digital Converter (ADC) for a list of ADC conversion commands).

When transitioning into ADC sleep state, care must be taken to ensure that the conversion command starts but does not complete before disabling the AHB clock. Perform the following step-by-step procedure:

1. Globally disable interrupts using “CLI” assembly language instruction
2. Initiate the conversion command.
3. Read back the conversion command (this ensures that the ADC command finite state machine acknowledges the command before disabling the AHB clock).
4. Disable AHB clock.
5. Globally re-enable interrupts using “STI” assembly language instruction

4.4.3 Standby State

Standby state is entered by stopping all clocks (except optionally the 32 kHz oscillator) midstream. Exit from standby state occurs when the real-time clock reaches terminal count or a comparator detects a reference voltage threshold crossing. Resumption of active state is typically within 2-5 µs of a threshold crossing depending on edge polarity and whether a high-speed or low-power comparator was used (Refer to Chapter 6. Timing Characteristics for more details). Like ADC sleep, care must be taken to ensure that the real-time clock or comparator event does not occur prior to disabling the AHB clock.

4.4.4 Retention State

Retention state is entered by lowering the core voltage to 1.35 V and stopping all clocks (except optionally the 32 kHz oscillator) midstream. Exit from retention state occurs when the real-time clock reaches terminal count or a comparator detects a reference voltage threshold crossing. Resumption of active state is typically within 800 µs of a threshold crossing (the relatively long wake-up time is needed in order to raise the core voltage to 1.8 V and ensure that the voltage regulator is in regulation). Like ADC sleep and standby, care must be taken to ensure that the real-time clock or comparator event does not occur prior to disabling the AHB clock.

Since entering retention state requires a very specific sequence of actions by software, a helper function is provided in ROM to simplify retention state entry.

4.5 Central Processing Unit (CPU)

The MCU is built around a 32-bit Harvard CISC CPU. Other features and benefits include:

- Single-issue, in-order 5-stage pipeline.
- Backward taken, forward not taken branch prediction.
- 32-bit data memory width.
- 128-bit instruction memory width.
- Single-cycle barrel shifter.
- Two-cycle multiplier.
- Multi-cycle hardware divider.
- JTAG debugging.
- Integrated PIC.
- Integrated 32-bit timer.

4.5.1 Programmable Interrupt Controller (PIC)

The MCU's CPU has an integrated PIC with a typical latency of 21 CPU clock cycles. Other features and benefits include:

- 16 individually maskable IRQ vectors.
- Individually programmable edge or level sensitivity.
- Programmable task priority threshold.

4.5.2 32-bit Timer

The MCU's CPU has an integrated 32-bit timer with programmable periodic or one shot modes. Other features and benefits include:

- Programmable vector can overlay peripheral IRQ vectors for software debug.
- Runs at CPU clock rate making it useful for code profiling as the CPU clock frequency changes.

4.5.3 JTAG Debug Controller

The MCU's CPU has an integrated JTAG debug controller with stream data transfer capability. Other features and benefits include:

- Start/stop run control.
- Single step.

- Instruction and data breakpoint registers.
- R/W peripheral, memory and core register content.

4.6 Flash

The MCU has 4 kB of data flash and 32 kB of code flash. Code flash occupies the address range 0x2000 0000 to 0x3FFF FFFF and is aliased throughout. It is accessible from both 128-bit code and 32-bit data busses. Data flash occupies the address range 0x4000 0000 to 0x5FFF FFFF and is aliased throughout. It is accessible only from the 32-bit data bus.

The user application and initialized data are stored in flash. The CPU executes in place directly from flash. The number of wait states required depends on the frequency:

- Zero wait states for clock frequencies up to 6.7 MHz.
- One wait state for clock frequencies up to 20 MHz.
- Two wait states for clock frequencies up to 33 MHz.

Flash cannot be written to directly from a CPU instruction. Helper functions in ROM assist the user application in storing data in flash. Attempting to write directly to flash generates a bus error causing a machine check exception. Instructions cannot be fetched from data flash. Attempting to do so generates a bus error causing a machine check exception.

Certain addresses in the upper page of data flash have been reserved for system configuration data. The following sections describe the system configuration data.

4.6.1 User Configuration Data

The MCU provides the user with a way to configure optional features of the bootstrap flow as well as enabling optional locks and CRCs for the various flash pages.

Table 6. User Configuration Data Stored In Upper Page of Data Flash

Address (hex)	Bits	Description
4000 0F80	15:0	Configuration Section Valid – a value of 0xAB8D indicates that the contents of this configuration section are valid. Any other value results in bootstrap terminating with JTAG enabled.
	17:16	Bootstrap Clock Frequency – this field configures the clock frequency at which the bootstrap procedure is executed. It is encoded thusly: 0 = 32 MHz 1 = 16 MHz 2 = 8 MHz 3 = 4 MHz
	31:18	Reserved

Address (hex)	Bits	Description
4000 0F84	7:0	Flash Instruction Page Lock – these bits control whether or not an instruction flash page is locked from erasing and writing using the built-in ROM utilities. Bit 0 corresponds to the 4 kB page beginning at address 0x2000 0000, bit 1 to the page beginning at address 0x2000 1000, and so on up to bit 7 which corresponds to the page beginning at address 0x2000 7000. When a bit is '0', the corresponding page is locked from erasing and writing.
	9:8	Flash Data Page Lock – these bits control whether or not a data flash page is locked from erasing and writing using the built-in ROM utilities. Bit 8 corresponds to the 2 kB page beginning at address 0x4000 0000 and bit 9 to the page beginning at address 0x4000 0800. When a bit is '0', the corresponding page is locked from erasing and writing.
	15:10	Reserved
	23:16	Erase Flash on Bootstrap Error – this field informs the bootstrap procedure how to proceed if there is an error. Any value other than 0xFF results in flash erasure prior to enabling JTAG. A value of 0xFF results in JTAG being enabled without flash erasure. **NOTE:** The global configuration section is never erased.
	31:24	Enable JTAG – this field informs the bootstrap procedure whether or not to enable JTAG prior to executing to the user program. A value of 0xFF results in JTAG being enabled just prior to executing the user program. Any value other than 0xFF results in executing the user program with JTAG disabled. Note that the user program can enable JTAG at any point after bootstrap.
4000 0F88	7:0	Flash Instruction Page CRC Disable – these bits control whether or not an instruction flash page is validated using CRC before the user program is executed. Bit 0 corresponds to the 4 kB page beginning at address 0x2000 0000, bit 1 to the page beginning at address 0x2000 1000, and so on up to bit 7 which corresponds to the page beginning at address 0x2000 7000. When a bit is '1', the corresponding page is not validated.
	9:8	Flash Data Page CRC Disable – these bits control whether or not a data flash page is validated using CRC before the user program is executed. Bit 8 corresponds to the 2 kB page beginning at address 0x4000 0000 and bit 9 to the page beginning at address 0x4000 0800. When a bit is '1', the corresponding page is not validated.
	31:10	Reserved
40000F8C	15:0	Flash Instruction Page 0 CRC – when the CRC validation for page 0 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.
	31:16	Flash Instruction Page 1 CRC – when the CRC validation for page 1 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled
4000 0F90	15:0	Flash Instruction Page 2 CRC – when the CRC validation for page 0 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.

Address (hex)	Bits	Description
	31:16	Flash Instruction Page 3 CRC – when the CRC validation for page 1 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.
4000 0F94	15:0	Flash Instruction Page 4 CRC – when the CRC validation for page 0 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.
	31:16	Flash Instruction Page 5 CRC – when the CRC validation for page 1 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.
4000 0F98	15:0	Flash Instruction Page 6 CRC – when the CRC validation for page 0 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.
	31:16	Flash Instruction Page 7 CRC – when the CRC validation for page 1 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.
4000 0F9C	15:0	Flash Data Page 0 CRC – when the CRC validation for page 0 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.
	31:16	Flash Data Page 1 CRC – when the CRC validation for page 1 is enabled, the calculated CRC must equal this value. A mismatch results in bootstrap terminating with JTAG enabled.
4000 0FA0 – 4000 0FBC	31:0	Reserved

4.6.2 Global Configuration

The MCU provides a non-volatile storage area for factory specific configuration information. Currently, only the oscillator trim code is stored here. The flash utilities provided in ROM will not allow the user to overwrite this information. However, it is possible to overwrite this information by directly accessing the flash controller. The flash controller is password protected to prevent accidental flash corruption

Table 7. Global Configuration Data Stored In Upper Page of Data Flash

Address (hex)	Bits	Description
4000 0FC0	7:0	Version – this field informs the bootstrap procedure which version of configuration section is in use. Since the MCU is the first generation in a series, this field is not currently used.
	15:8	Reserved
	31:16	Configuration Section Valid – a value of 0x5CAB indicates that the contents of this configuration section are valid. Any other value results in bootstrap terminating with JTAG enabled.

Address (hex)	Bits	Description
4000 0FC4	9:0	Silicon Oscillator Trim Code – this value trims the silicon oscillator to the desired frequency. The frequency is a monotonic function of this value. The oscillator is trimmed before configuring the bootstrap frequency.
	31:10	Reserved
4000 0FC8 – 4000 0FFC	31:0	Reserved

4.7 ROM

The MCU has 8 kB of zero latency, zero wait state ROM. This memory is accessible from both the 128-bit code and 32-bit data busses. It occupies the address range 0x0000 0000 to 0x1FFF FFFF and is aliased throughout. In addition to the bootstrap procedure, it contains the following helper functions:

- CCITT CRC-16.
- Flash mass erase.
- Flash page erase.
- Flash page write.
- Enter retention state.
- Calibrate oscillator.
- AES decrypt.
- AES encrypt.
- AES expand key.

ROM cannot be written. Attempting to write directly to ROM generates a bus error causing a machine check exception.

4.8 SRAM

The MCU has 8 kB of zero latency, zero wait state SRAM. This memory is accessible only from the 32-bit data bus. It occupies the address range 0x6000 0000 to 0x7FFF FFFF and is aliased throughout. Instructions cannot be fetched from SRAM. Attempting to do so generates a bus error, which causes a machine check exception.

4.9 Peripheral Bus Interconnects

The MCU uses two peripheral busses from the AMBA family: (1) AHB-Lite and (2) APB. These are memory mapped into the upper half of the CPU's 4 GB address range. This address range is strongly ordered, meaning that transactions will not be reordered or

duplicated. They occur in the order that they appear in the executable binary image. Instructions cannot be fetched from the peripheral busses. Attempting to do so generates a bus error causing a machine check exception.

4.9.1 AHB-Lite

This 32-bit bus complies with the AMBA 3 AHB-Lite Protocol Specification (ARM Limited, 2006). AHB-Lite supports zero latency, zero wait state transfers between a single master and many peripherals. Transfer rates can approach 132 MBps. It occupies the address range 0x8000 0000 to 0x8FFF FFFF. Its clock runs at the CPU clock frequency except that when the CPU is in halt state, the clock is gated off.

4.9.2 APB

This 32-bit bus complies with the AMBA 3 APB Protocol Specification (ARM Limited, 2004). Transfer rates over APB vary by peripheral, but cannot exceed 44 MBps. It occupies the address range 0x9000 0000 to 0x9FFF FFFF. Its clock runs at the AHB clock frequency except that software can gate it off independent of the AHB clock, effectively shutting down all APB peripherals.

4.10 Serial Peripheral Interface (SPI)

The MCU has two independent SPI peripherals: (1) master and (2) slave. These can both be used simultaneously. A variety of protocols and modes are supported making it easy to connect with most popular SPI peripherals. Software can choose from Motorola SPI*, Texas Instruments Synchronous Serial Protocol (SSP)* or National Semiconductor Microwire* transfer types on a per transfer basis. Software can also choose from transmit only, receive only, transmit-receive, and EEPROM transfer modes. Other features and benefits include:

- Master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow interrupts. All can be masked independently.
- Interrupt or polled-mode operation.
- Multi-master contention detection informs the processor of multiple serial-master accesses on the serial bus.
- Programmable delay on the sample time of the received serial data bit (MISO). This can be used to compensate for round trip delays that could otherwise limit baud rate.
- Programmable baud rates up to 16.5 Mbps.
- Programmable word size from 4-16 bits.
- Eight word transmit and receive FIFO buffers with programmable interrupt thresholds.

- Four automatically generated slave-select outputs on SPI master.
- Independent SPI clock allows CPU clock frequency changes without affecting in-progress transfers.
- Component version register.

Figure 7 through Figure 13 provides waveforms for the various protocols supported.

Figure 7. Motorola SPI Mode 00/10 Single Transfer

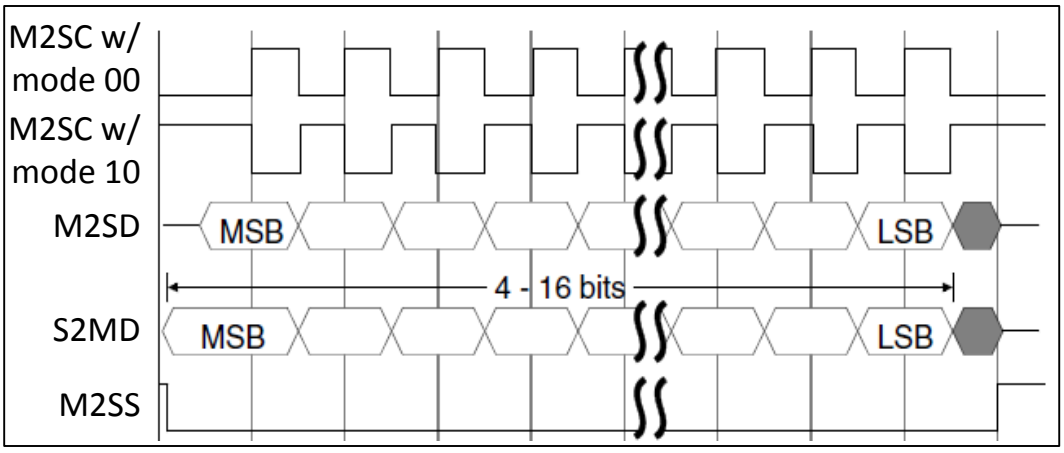


Figure 8. Motorola SPI Mode 00/10 Continuous Transfer

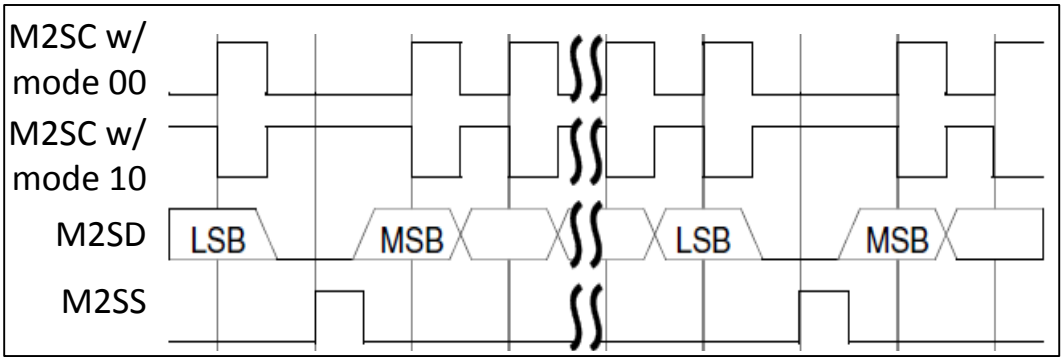


Figure 9. Motorola SPI Mode 01/11 Single Transfer

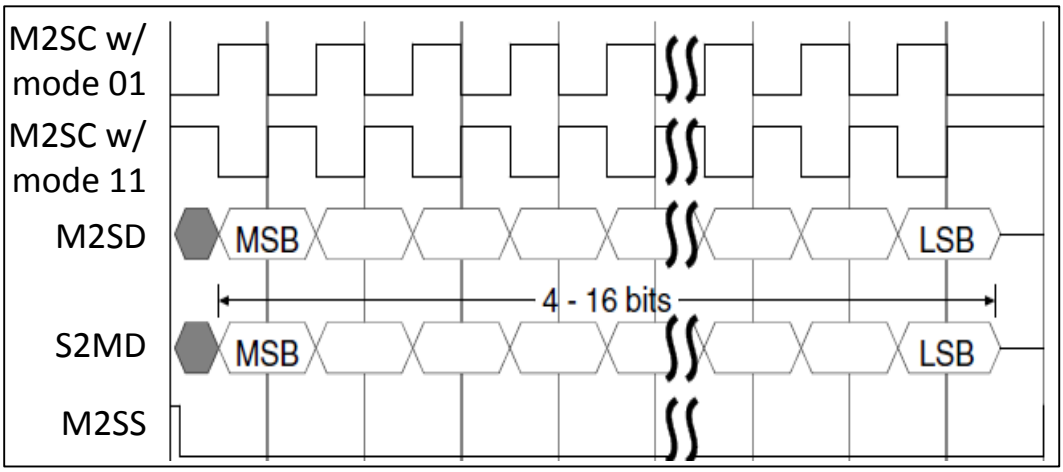


Figure 10. Motorola SPI Mode 01/11 Continuous Transfer

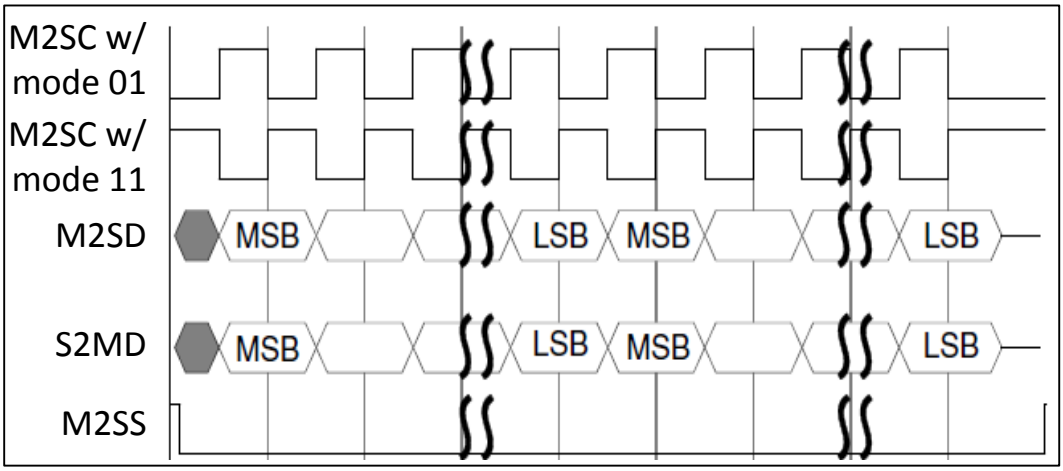


Figure 11. Texas Instruments Synchronous Serial Protocol (SSP) Continuous Transfer

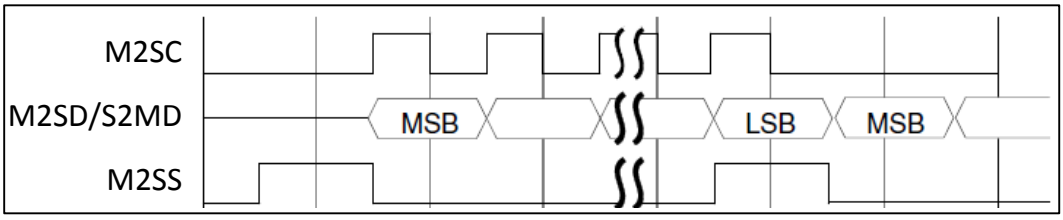


Figure 12. National Semiconductor Microwire Single Transfer

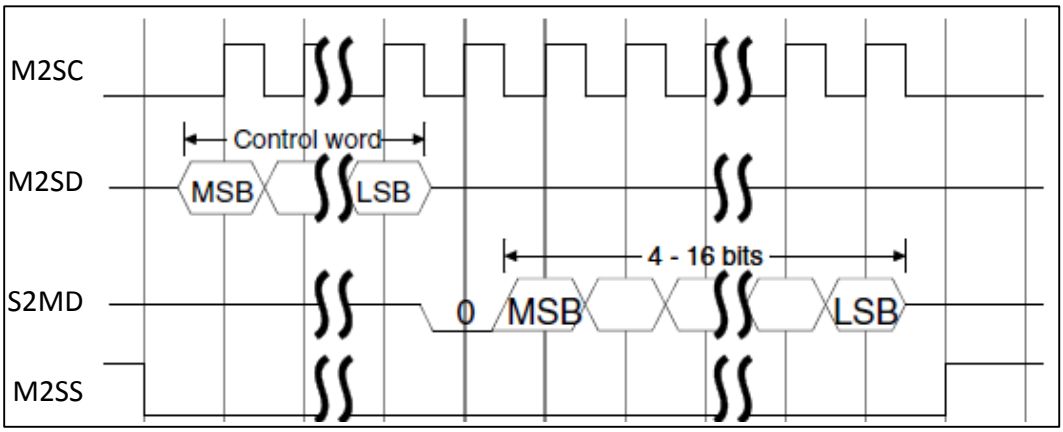
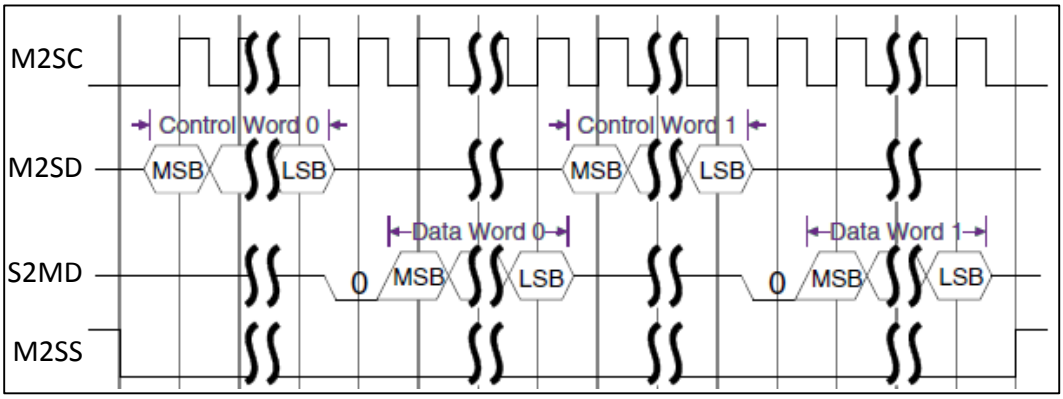


Figure 13. National Semiconductor Microwire Continuous Transfer



4.11 I²C Bus

The MCU has an I²C peripheral interface that can be programmed as master or slave. It complies with the requirements for standard and fast operating modes as defined in the I²C Bus Specification (NXP Semiconductors, 2007). Other features and benefits include:

- Standard (up to 100 kbps) and fast (up to 400 kbps) modes.
- Programmable master or slave operation.
- Programmable 7- or 10-bit addressing with combined format transfers.
- Bulk transmit mode.
- Ignores CBUS addresses (an older ancestor of I²C that used to share the I²C bus).
- Eight-byte transmit and receive FIFOs with programmable threshold levels.
- Eleven independently maskable interrupts.

- Interrupt or polled-mode operation.
- Handles bit and byte waiting at all bus speeds.
- Programmable SDA hold time.
- Component version register.

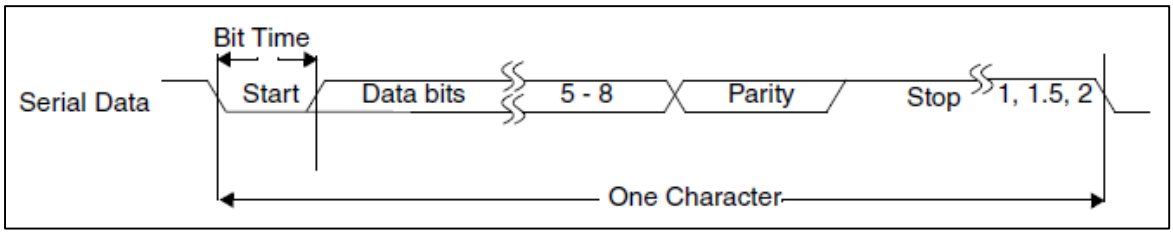
4.12 Universal Asynchronous Receiver/Transmitter (UART)

The MCU has two National Semiconductor 16550-compatible UARTs that can be used simultaneously. They support hardware handshaking and baud rates up to 2 Mbaud. Other features and benefits include:

- 16 characters transmit and receive FIFOs with programmable interrupt thresholds.
- Programmable FIFO enable/disable.
- Additional FIFO status registers.
- Shadow registers to reduce software overhead.
- Software programmable reset.
- Loopback mode that enables software testing of modem control features.
- Busy functionality helps to safe guard against errors if the LCR, DLL, and/or DLH registers are changed during a transaction even though they should only be set during initialization.
- Independently controlled modem and status lines.
- False start bit detection.
- Component version register.

Figure 14 provides the format of a UART transmit/receive character.

Figure 14. Format of UART Transmit/Receiver Data



4.13 General Purpose Input/Output (GPIO)

The MCU has 24 general purpose digital I/O buffers that provide software with direct access to pins. Each GPIO can be programmed as input with optional pull-up, push-pull output, open drain output with optional internal pull-up, or bidirectional. GPIO are multiplexed with other functions (refer to Figure 1). As inputs, they can be edge or level sensitive. As outputs, they have programmable slew rate control. Other features and benefits include:

- Separate output data, input data and data direction registers.
- Each pin independently controlled.
- Independently-maskable interrupts per pin.
- Built-in synchronization registers for edge detection.
- Component version register.

4.14 Real-time Clock

The MCU has a 32-bit real-time clock driven by the 32 kHz oscillator that can be used to keep track of time even when all other system clocks are disabled or the core voltage is reduced to retention levels. Other features and benefits include:

- Programmable match register to trigger an interrupt at the specified time.
- Programmable counter load register to initialize the current time.
- Programmable wrap mode controls when the counter wraps to zero – when match time is reached or when all ones count is reached.
- Maskable interrupt will automatically restart the system oscillator when match time is reached.
- Component version register.

4.15 Watchdog Timer

The MCU has a 32-bit watchdog timer driven by *apb_clk* that can be used to reset the microcontroller in the event of a software error that makes the system unresponsive. Other features and benefits include:

- Programmable timeout mode – reset on timeout or interrupt on first timeout; then reset on second timeout.
- Programmable timeout period.
- Write inhibit after enablement to prevent accidental disabling or changing of timeout period.
- Component version register.

4.16 General Purpose Timers

The MCU has two 32-bit general purpose timers in addition to the CPU's built-in timer. These timers are driven by independent clocks allowing CPU clock frequency changes without affecting timer rate. Other features and benefits include:

- Independent load count registers.
- Independent current count registers.
- Independently maskable interrupts.
- Programmable wrap mode controls what value the counter wraps to after counting down to zero – all ones or the value on the load count register.
- Component version register.

4.17 Analog to Digital Converter (ADC)

The MCU has a 2.4 MSps 12-bit SAR ADC controlled by two finite state machines (FSM): one for power management and the second for conversion mode. These two FSMs minimize power consumption and greatly simplify use of the ADC. Other features and benefits include:

- Independent ADC clock allowing CPU clock disabling or frequency changes without affecting ADC sample rate.
- Five power modes:
  1. Deep power down.
  2. Power down.
  3. Standby.
  4. Operational with calibration.
  5. Operational without calibration.
- Six conversion commands:
  1. Start single conversion.
  2. Start continuous conversion.
  3. Reset calibration.
  4. Start calibration.
  5. Load calibration.
  6. Stop continuous conversion.
- Programmable 6, 8, 10 or 12-bit resolution.
- Programmable sample rate:
  - up to 2.4 MSps at 12-bit resolution.
  - up to 2.8 MSps at 10-bit resolution.
  - up to 3.3 MSps at 8-bit resolution.

  - up to 4.2 MSps at 6-bit resolution.
- Programmable sample window for high impedance sources.
- Programmable 32-entry arbitrary channel scan sequence table.
- Maskable interrupt will automatically enable the CPU clock when conversions are complete.
- 32-entry sample FIFO with programmable threshold.
- Automatic offset calibration.
- Pre-load of calibration coefficients for fast resumption after power down.

4.18 Comparators

The MCU has six high-speed comparators (AI[0:5]) and thirteen low-power comparators (AI[6:18]). The high-speed comparators offer 1.6 MHz typical bandwidth while the low-power comparators offer 360 nA typical static leakage current. Example uses include amplitude shift key demodulation with an external envelope detector or wake-up from analog threshold crossings or digital signals. Other features and benefits include:

- Independently maskable interrupts will automatically restart the system oscillator when a threshold crossing is detected during standby or retention states.
- Independent polarity control for each comparator.
- Independent power control for each comparator.
- Independent reference select – external via AR pin or internal 0.95 V.

§

5.0 Electrical Characteristics

The characteristics provided in the following sections are preliminary and subject to change. The parameters have been measured on a limited quantity of TTT, TSS and TFF skew material under the temperature and voltage conditions given. The parameter values may change as additional data becomes available.

Table 8. Absolute Maximum Ratings

Parameter	Condition	Min	Max	Unit
Supply voltage	V_{PVDD}=V_{AVDD}=V_{IOVDD}	-0.5	3.63	V
	V_{DVDD} with V_{REN}=V_{SS}	-0.5	1.98	V
Supply differential voltage	V_{PVDD}-V_{AVDD} V_{PVDD}-V_{IOVDD} V_{AVDD}-V_{IOVDD}	-0.5	0.5	V
Voltage at XTALI[0] or XTALI[1]	-	-0.5	V_{DVDD}+0.5	V
Voltage at any other pin[1]	V_{PVDD}=V_{AVDD}=V_{IOVDD}	-0.5	V_{IOVDD}+0.5	V
Storage temperature	-	-55	150	°C

[1]LX must be connected as shown in Figure 6 or damage to the device may result.

Table 9. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage with VR enabled	V_{PVDD} with V_{VREN}=V_{PVDD}	1.82		3.63	V
Supply voltage with VR disabled	V_{PVDD}=V_{AVDD}=V_{IOVDD} with V_{VREN}=V_{SS}	1.62		3.63	V
	V_{DVDD} with V_{VREN}=V_{SS}	1.62	1.80	1.98	V
Operating temperature	Free air	-40		85	°C
Digital input low to high threshold point	3.00 V≤V_{IOVDD}≤3.63 V without pull-up	1.52	1.66	1.83	V
	2.25 V≤V_{IOVDD}≤2.75 V without pull-up	1.23	1.36	1.50	V
	1.62 V≤V_{IOVDD}≤1.98 V without pull-up	0.96	1.09	1.17	V
Digital input high to low threshold point	3.00 V≤V_{IOVDD}≤3.63 V without pull-up	1.30	1.43	1.57	V
	2.25 V≤V_{IOVDD}≤2.75 V without pull-up	0.95	1.05	1.16	V
Digital input high to low threshold point (Cont.)	1.62 V≤V_{IOVDD}≤1.98 V without pull-up	0.63	0.79	0.90	V

Parameter	Condition	Min	Typ	Max	Unit
Input leakage	Without pull-up	-10		10	mA
Digital output source current with slew rate control set for slow	3.00 V≤V_{IOVDD}≤3.63 V, V_O=2.4 V	-22.0	-34.8	-53.4	mA
	2.25 V≤V_{IOVDD}≤2.75 V, V_O=1.7 V	-14.6	-24.3	-37.5	mA
	1.62 V≤V_{IOVDD}≤1.98 V, V_O=1.35 V	-5.1	-10.3	-18.1	mA
Digital output source current with slew rate control set for fast	3.00 V≤V_{IOVDD}≤3.63 V, V_O=2.4 V	-29.6	-46.8	-71.6	mA
	2.25 V≤V_{IOVDD}≤2.75 V, V_O=1.7 V	-19.8	-32.9	-50.8	mA
	1.62 V≤V_{IOVDD}≤1.98 V, V_O=1.35 V	-7.2	-14.1	-24.6	mA
Digital output sink current with slew rate control set for slow	3.00 V≤V_{IOVDD}≤3.63 V, V_O=0.4 V	17.0	19.6	29.1	mA
	2.25 V≤V_{IOVDD}≤2.75 V, V_O=0.7 V	17.5	20.1	30.0	mA
	1.62 V≤V_{IOVDD}≤1.98 V, V_O=0.45 V	7.2	9.5	15.1	mA
Digital output sink current with slew rate control set for fast	3.00 V≤V_{IOVDD}≤3.63 V, V_O=0.4 V	23.8	25.4	34.7	mA
	2.25 V≤V_{IOVDD}≤2.75 V, V_O=0.7 V	23.1	24.8	37.6	mA
	1.62 V≤V_{IOVDD}≤1.98 V, V_O=0.45 V	10.2	12.4	19.4	mA

Note: Attempting to operate the MCU below the recommended supply voltages specified in Table 9 may result in flash erasure.

Table 10. System Power Consumption

Parameter	Condition	Min	Typ	Max	Unit
Total active power[1] with VR enabled P_{AVDD}+P_{PVDD}+P_{IOVDD}	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{CPU}=32 MHz, f_{ADC}=0	–	25.3	30.5	mW
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{CPU}=32 MHz, f_{ADC}=0	–	25.2	27.4	mW
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{CPU}=32 MHz, f_{ADC}=0	–	22.6	25.6	mW
	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{CPU}=1 MHz, f_{ADC}=0	–	1.66	1.89	mW
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{CPU}=1 MHz, f_{ADC}=0	–	1.45	1.64	mW
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{CPU}=1 MHz, f_{ADC}=0	–	1.35	1.40	mW

Parameter	Condition	Min	Typ	Max	Unit
Total halt power[2] with VR enabled $P_{AVDD}+P_{PVDD}+P_{IOVDD}$	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{CPU}=32 MHz, f_{ADC}=0	–	7.55	9.91	mW
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{CPU}=32 MHz, f_{ADC}=0	–	7.27	8.90	mW
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{CPU}=32 MHz, f_{ADC}=0	–	6.80	9.24	mW
	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{CPU}=1 MHz, f_{ADC}=0	–	1.03	1.15	mW
Total halt power2 with VR enabled $P_{AVDD}+P_{PVDD}+P_{IOVDD}$ (Cont.)	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{CPU}=1 MHz, f_{ADC}=0	–	0.88	0.92	mW
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{CPU}=1 MHz, f_{ADC}=0	–	0.78	0.87	mW
ADC sleep current $I_{AVDD}+I_{PVDD}+I_{IOVDD}$	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=32 MHz, f_{CPU}=0	–	1.45	1.56	mA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=32 MHz, f_{CPU}=0	–	1.59	1.69	mA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=32 MHz, f_{CPU}=0	–	1.84	1.94	mA
	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=4 MHz, f_{CPU}=0	–	350	386	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=4 MHz, f_{CPU}=0	–	376	419	µA
	1.82V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18V, -40≤T≤85°C, f_{ADC}=4 MHz, f_{CPU}=0	–	422	490	µA
Standby current With RTC without comparator $I_{AVDD}+I_{PVDD}+I_{IOVDD}$	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	4.8	11.8	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	4.7	11.8	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	4.7	11.8	µA
Retention current With RTC without comparator $I_{AVDD}+I_{PVDD}+I_{IOVDD}$	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	3.0	9.5	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	2.9	9.5	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	2.9	9.5	µA

Parameter	Condition	Min	Typ	Max	Unit
Standby current Without RTC with low-power comparator $I_{AVDD}+I_{PVDD}+I_{IOVDD}$	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	2.1	8.0	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	2.0	8.0	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	2.0	8.0	µA
Retention current Without RTC with low-power comparator $I_{AVDD}+I_{PVDD}+I_{IOVDD}$	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	1.6	7.0	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	1.5	7.0	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=0, f_{CPU}=0	–	1.5	7.0	µA

Notes:

1. Active power is measured while executing a 64-point FFT with ADC and all comparators powered off, all branch clocks disabled, and all peripherals inactive.
2. Halt power is measured while CPU is halted with ADC and all comparators powered off, all branch clocks disabled, and all peripherals inactive.

Table 11. Comparator Current Consumption

Parameter	Condition	Min	Typ	Max	Unit
High-speed comparator static current (I_{AVDD})	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{IN}=0	–	5.7	7.1	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{IN}=0	–	5.7	7.0	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{IN}=0	–	5.7	7.0	µA
Low-power comparator static current (I_{AVDD})	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{IN}=0	–	0.4	0.5	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{IN}=0	–	0.4	0.5	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{IN}=0	–	0.4	0.5	µA
High-speed comparator dynamic current (I_{AVDD})	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{IN}=40 mV_{PP}	–	5.9	7.8	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.7 5V, -40≤T≤85°C, f_{IN}=600 kHz, V_{IN}=40 mV_{PP}	–	5.8	7.3	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{IN}=40 mV_{PP}	–	5.8	7.2	µA

Parameter	Condition	Min	Typ	Max	Unit
Low-power comparator dynamic current (I_{AVDD})	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{IN}=40 mV_{PP}	–	1.1	1.8	µA
Low-power comparator dynamic current (IAVDD) (Cont.)	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{IN}=40 mV_{PP}	–	0.5	1.0	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{IN}=40 mV_{PP}	–	0.4	1.0	µA

Table 12. Oscillator Current Consumption

Parameter	Condition	Min	Typ	Max	Unit
Silicon oscillator current consumption (I_{DVDD})	1.2 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=4 MHz	–	171	182	µA
	1.2 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=8 MHz	–	177	189	µA
	1.2 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=16 MHz	–	308	328	µA
	1.2 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=32 MHz	–	448	471	µA
Crystal oscillator current consumption (I_{DVDD})	1.2 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=33 MHz	–	905	1051	µA
RTC oscillator current consumption (I_{DVDD})	1.2 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=32 kHz	–	3.4	3.8	µA

Table 13. ADC Current Consumption

Parameter	Condition	Min	Typ	Max	Unit
ADC standby current (I_{AVDD})	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=0	–	18	21	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=0	–	18	21	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=0	–	17	20	µA
ADC normal current (I_{AVDD})	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=32 MHz	–	33	38	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=32 MHz	–	32	36	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=32 MHz	–	31	35	µA
ADC calibration current (I_{AVDD})	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=32 MHz	–	101	117	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=32 MHz	–	100	115	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=32 MHz	–	99	114	µA
ADC active current (I_{AVDD})	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=32 MHz, R=2.3 MSps	–	512	581	µA

Parameter	Condition	Min	Typ	Max	Unit
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=32 MHz, R=2.3 MSps	–	441	505	µA
ADC active current (I_{AVDD}) (Cont.)	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=32 MHz, R=2.3 MSps	–	381	436	µA
	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C, f_{ADC}=32 MHz, R=4.0 MSps	–	677	775	µA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C, f_{ADC}=32 MHz, R=4.0 MSps	–	561	650	µA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C, f_{ADC}=32 MHz, R=4.0 MSps	–	466	532	µA

Table 14. Low-power Comparator Hysteresis

Parameter	Condition	Min	Typ	Max	Unit
Low-power comparator hysteresis with low external reference voltage and low frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	5.0	6.1	8.2	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	3.4	6.1	8.3	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	4.2	6.1	8.3	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, V_{AR}=0V	3.0	5.7	7.9	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=1 kHz, V_{AR}=0V	5.6	7.2	8.1	mV
Low-power comparator hysteresis with low external reference voltage and median frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, V_{AR}=0V	9.3	10.7	14.5	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, V_{AR}=0V	7.1	9.7	12.8	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, V_{AR}=0V	6.0	9.2	13.3	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=35 kHz, V_{AR}=0V	4.0	7.9	11.3	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=35 kHz, V_{AR}=0V	9.1	12.0	15.0	mV
Low-power comparator hysteresis with low external reference voltage and high frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=0V	11.9	14.0	20.6	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=0V	10.4	12.8	15.7	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=0V	7.4	11.4	15.6	mV

Parameter	Condition	Min	Typ	Max	Unit
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$ V, $V_{DVDD}=1.2$ V, T=-40°C, $f_{IN}=70$ kHz, $V_{AR}=0V$	4.7	9.2	13.7	mV
Low-power comparator hysteresis with low external reference voltage and high frequency (Cont.)	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=70$ kHz, $V_{AR}=0V$	12.3	14.8	19.6	mV
Low-power comparator hysteresis with internal reference voltage and low frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=0V$	2.7	6.0	8.9	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=0V$	2.6	4.4	9.1	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=0V$	2.6	4.1	9.1	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$ V, $V_{DVDD}=1.2$ V, T=-40°C, $f_{IN}=1$ kHz, $V_{AR}=0V$	2.7	3.7	5.6	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=1$ kHz, $V_{AR}=0V$	5.5	7.5	8.9	mV
Low-power comparator hysteresis with internal reference voltage and median frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=35$ kHz, V_{REF}≈0.95 V	6.9	10.4	19.0	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=35$ kHz, V_{REF}≈0.95 V	4.7	7.5	19.8	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=35$ kHz, V_{REF}≈0.95 V	4.3	6.9	14.9	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$ V, $V_{DVDD}=1.2$ V, T=-40°C, $f_{IN}=35$ kHz, V_{REF}≈0.95 V	6.9	10.1	16.3	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=35$ kHz, V_{REF}≈0.95 V	9.0	13.6	16.7	mV
Low-power comparator hysteresis with internal reference voltage and high frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=70$ kHz, V_{REF}≈0.95 V	8.9	14.6	30.3	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=70$ kHz, V_{REF}≈0.95 V	6.6	10.5	28.2	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=70$ kHz, V_{REF}≈0.95 V	5.5	9.2	22.6	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$ V, $V_{DVDD}=1.2$ V, T=-40°C, $f_{IN}=70$ kHz, V_{REF}≈0.95 V	13.1	18.0	24.4	mV

Parameter	Condition	Min	Typ	Max	Unit
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=70 kHz, V_{REF}≈0.95 V	12.0	21.6	26.2	mV
Low-power comparator hysteresis with high external reference voltage and low frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	2.3	3.3	6.5	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	2.5	3.3	5.6	mV
Low-power comparator hysteresis with high external reference voltage and low frequency (Cont,)	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	2.3	3.6	5.2	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	2.7	3.1	3.9	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	3.2	3.8	4.9	mV
Low-power comparator hysteresis with high external reference voltage and median frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, $V_{AR}=V_{AVDD}$	4.8	7.2	16.9	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, $V_{AR}=V_{AVDD}$	4.1	6.0	13.8	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, $V_{AR}=V_{AVDD}$	4.6	5.8	12.9	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=35 kHz, $V_{AR}=V_{AVDD}$	3.7	4.8	5.8	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=35 kHz, $V_{AR}=V_{AVDD}$	5.2	8.3	9.7	mV
Low-power comparator hysteresis with high external reference voltage and high frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, $V_{AR}=V_{AVDD}$	7.9	11.2	17.4	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, $V_{AR}=V_{AVDD}$	6.1	9.2	15.8	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, $V_{AR}=V_{AVDD}$	5.3	8.7	13.7	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=70 kHz, $V_{AR}=V_{AVDD}$	5.3	6.5	8.4	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=70 kHz, $V_{AR}=V_{AVDD}$	9.4	10.9	14.7	mV

Table 15. High-speed Comparator Hysteresis

Parameter	Condition	Min	Typ	Max	Unit
High-speed comparator hysteresis with low external	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	2.1	3.9	4.7	mV

Parameter	Condition	Min	Typ	Max	Unit
reference voltage and low frequency	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	2.2	3.8	4.9	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	2.2	3.8	4.8	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, V_{AR}=0V	1.7	3.3	3.7	mV
High-speed comparator hysteresis with low external reference voltage and low frequency (Cont.)	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=1 kHz, V_{AR}=0V	2.1	3.9	4.5	mV
High-speed comparator hysteresis with low external reference voltage and median frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=0V	3.9	5.4	7.3	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=0V	4.0	5.0	6.9	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=0V	4.0	4.7	6.2	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62V, V_{DVDD}=1.2V, T=-40°C, f_{IN}=300kHz, V_{AR}=0V	2.0	4.2	5.3	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63V, V_{DVDD}=1.2V, T=85°C, f_{IN}=300kHz, V_{AR}=0V	5.2	5.9	7.0	mV
High-speed comparator hysteresis with low external reference voltage and high frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=0V	4.7	6.5	9.2	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=0V	4.7	6.1	8.7	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=0V	4.2	5.6	7.4	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=600 kHz, V_{AR}=0V	2.4	5.0	6.2	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=600 kHz, V_{AR}=0V	6.2	6.9	7.5	mV
High-speed comparator hysteresis with internal reference voltage and low frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	3.0	3.7	6.5	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	3.1	4.2	5.8	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	3.1	4.1	6.6	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, V_{AR}=0V	2.2	3.8	4.8	mV

Parameter	Condition	Min	Typ	Max	Unit
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=1$ kHz, $V_{AR}=0$V	3.9	4.4	5.1	mV
High-speed comparator hysteresis with internal reference voltage and median frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=300$ kHz, V_{REF}≈0.95 V	4.4	5.7	12.9	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=300$ kHz, V_{REF}≈0.95 V	4.9	5.7	12.4	mV
High-speed comparator hysteresis with internal reference voltage and median frequency (Cont.)	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=300$ kHz, V_{REF}≈0.95 V	4.2	5.3	9.8	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$ V, $V_{DVDD}=1.2$ V, T=-40°C, $f_{IN}=300$ kHz, V_{REF}≈0.95 V	3.7	5.0	5.9	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=300$ kHz, V_{REF}≈0.95 V	6.4	7.5	10.0	mV
High-speed comparator hysteresis with internal reference voltage and high frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=600$ kHz, V_{REF}≈0.95 V	5.6	7.8	21.6	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=600$ kHz, V_{REF}≈0.95 V	6.1	7.4	23.8	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=600$ kHz, V_{REF}≈0.95 V	5.4	6.2	11.8	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$V, $V_{DVDD}=1.2$V, T=-40°C, $f_{IN}=600$kHz, V_{REF}≈0.95V	5.6	7.2	12.4	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=600$ kHz, V_{REF}≈0.95 V	7.4	10.4	14.0	mV
High-speed comparator hysteresis with high external reference voltage and low frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=V_{AVDD}$	2.6	4.1	7.6	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=V_{AVDD}$	2.2	4.2	6.9	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=V_{AVDD}$	2.6	4.2	8.5	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$ V, $V_{DVDD}=1.2$ V, T=-40°C, $f_{IN}=1$ kHz, $V_{AR}=V_{AVDD}$	3.1	3.7	4.6	mV

Parameter	Condition	Min	Typ	Max	Unit
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=1$ kHz, $V_{AR}=V_{AVDD}$	4.2	4.6	5.2	mV
High-speed comparator hysteresis with high external reference voltage and median frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=300$ kHz, $V_{AR}=V_{AVDD}$	4.1	6.2	9.5	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=300$ kHz, $V_{AR}=V_{AVDD}$	4.7	5.9	8.3	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=300$ kHz, $V_{AR}=V_{AVDD}$	4.6	5.3	7.9	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$ V, $V_{DVDD}=1.2$ V, T=-40°C, $f_{IN}=300$ kHz, $V_{AR}=V_{AVDD}$	4.2	4.8	5.9	mV
High-speed comparator hysteresis with high external reference voltage and median frequency (Cont.)	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=300$ kHz, $V_{AR}=V_{AVDD}$	7.2	8.7	10.3	mV
High-speed comparator hysteresis with high external reference voltage and high frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=600$ kHz, $V_{AR}=V_{AVDD}$	6.4	8.5	11.0	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=600$ kHz, $V_{AR}=V_{AVDD}$	6.1	7.8	9.9	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=600$ kHz, $V_{AR}=V_{AVDD}$	5.2	6.7	9.8	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62$ V, $V_{DVDD}=1.2$ V, T=-40°C, $f_{IN}=600$ kHz, $V_{AR}=V_{AVDD}$	5.3	6.1	7.2	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63$ V, $V_{DVDD}=1.2$ V, T=85°C, $f_{IN}=600$ kHz, $V_{AR}=V_{AVDD}$	8.2	9.5	12.9	mV

Table 16. Low-power Comparator Input Offset Using External Voltage Reference

Parameter	Condition	Min	Typ	Max	Unit
Low-power comparator input offset using low external reference voltage and low frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=0$V	-13.2	0.9	11.1	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=0$V	-13.1	-0.4	9.6	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, $f_{IN}=1$ kHz, $V_{AR}=0$V	-13.0	-0.4	9.8	mV

Parameter	Condition	Min	Typ	Max	Unit
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, V_{AR}=0V	-14.2	-2.2	4.6	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=1 kHz, V_{AR}=0V	-10.8	-0.5	10.0	mV
Low-power comparator input offset using low external reference voltage and median frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, V_{AR}=0V	-17.1	-0.1	10.9	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, V_{AR}=0V	-14.2	-1.4	9.5	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, V_{AR}=0V	-13.7	-0.9	9.6	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=35 kHz, V_{AR}=0V	-15.5	-2.4	6.5	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=35 kHz, V_{AR}=0V	-11.3	-1.5	8.6	mV
Low-power comparator input offset using low external reference voltage and high frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=0V	-18.5	-1.1	11.0	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=0V	-15.9	-2.0	9.5	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=0V	-14.7	-1.3	9.4	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=70 kHz, V_{AR}=0V	-16.0	-2.6	6.6	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=70 kHz, V_{AR}=0V	-10.4	-1.6	11.7	mV
Low-power comparator input offset using high external reference voltage and low frequency	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	-14.6	-1.1	11.0	mV
	2.25 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤2.75 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	-12.9	-1.0	10.1	mV
	1.62 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤1.98 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	-11.6	-0.9	10.2	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	-3.8	1.1	5.9	mV
	$V_{PVDD}=V_{AVDD}=V_{IOVDD}$=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=1 kHz, $V_{AR}=V_{AVDD}$	-13.8	-0.3	10.5	mV
Low-power comparator input offset using high external	3.00 V≤$V_{PVDD}=V_{AVDD}=V_{IOVDD}$≤3.63 V, 1.62 V≤$V_{DVDD}$ ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, $V_{AR}=V_{AVDD}$	-14.2	0.5	11.3	mV

Parameter	Condition	Min	Typ	Max	Unit
reference voltage and median frequency	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, V_{AR}=V_{AVDD}	-12.7	-0.1	11.3	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=35 kHz, V_{AR}=V_{AVDD}	-11.3	-0.7	11.7	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=35 kHz, V_{AR}=V_{AVDD}	-3.8	1.3	6.3	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=35 kHz, V_{AR}=V_{AVDD}	-14.2	1.0	11.2	mV
Low-power comparator input offset using high external reference voltage and high frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=V_{AVDD}	-14.9	1.4	13.5	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=V_{AVDD}	-12.1	0.2	13.1	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{AR}=V_{AVDD}	-10.9	-0.5	12.0	mV
Low-power comparator input offset using high external reference voltage and high frequency (Cont.)	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=70 kHz, V_{AR}=V_{AVDD}	-3.6	1.4	6.3	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=70 kHz, V_{AR}=V_{AVDD}	-14.2	2.0	11.3	mV

Table 17. High-speed Comparator Input Offset Using External Reference

Parameter	Condition	Min	Typ	Max	Volts
High-speed comparator input offset using low external reference voltage and low frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	-5.6	0.2	5.5	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	-5.5	0.6	4.6	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	-5.1	0.7	4.4	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, V_{AR}=0V	-5.5	-0.2	4.8	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=1 kHz, V_{AR}=0V	-3.6	1.1	5.4	mV
High-speed comparator input offset using low external reference voltage and median frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=0V	-5.9	0.2	5.7	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=0V	-5.0	0.6	4.3	mV

Parameter	Condition	Min	Typ	Max	Volts
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=0V	-5.1	0.8	4.2	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62V, V_{DVDD}=1.2V, T=-40°C, f_{IN}=300kHz, V_{AR}=0V	-5.2	-0.2	4.5	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=300 kHz, V_{AR}=0V	-4.1	0.8	5.3	mV
High-speed comparator input offset using low external reference voltage and high frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=0V	-5.9	-0.4	5.5	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=0V	-5.1	0.5	5.5	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=0V	-5.9	0.9	5.2	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=600 kHz, V_{AR}=0V	-5.0	-0.2	4.3	mV
High-speed comparator input offset using low external reference voltage and high frequency (Cont.)	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=600 kHz, V_{AR}=0V	-4.2	0.6	5.1	mV
High-speed comparator input offset using high external reference voltage and low frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=V_{AVDD}	-5.4	-0.9	5.3	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=V_{AVDD}	-5.3	-0.8	4.4	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=V_{AVDD}	-4.9	-0.7	3.8	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, V_{AR}=V_{AVDD}	-5.4	0.1	3.9	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=1 kHz, V_{AR}=V_{AVDD}	-6.0	-0.1	3.3	mV
High-speed comparator input offset using high external reference voltage and median frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=V_{AVDD}	-5.3	-0.5	5.6	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=V_{AVDD}	-5.1	-0.6	5.0	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{AR}=V_{AVDD}	-4.7	-0.7	3.6	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=300 kHz, V_{AR}=V_{AVDD}	-4.7	0.1	3.6	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=300 kHz, V_{AR}=V_{AVDD}	-4.6	0.7	5.2	mV

Parameter	Condition	Min	Typ	Max	Volts
High-speed comparator input offset using high external reference voltage and high frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=V_{AVDD}	-5.2	-0.4	6.1	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=V_{AVDD}	-4.8	-0.4	5.7	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{AR}=V_{AVDD}	-4.7	-0.7	3.5	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=600 kHz, V_{AR}=V_{AVDD}	-4.5	0.1	3.7	mV
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=600 kHz, V_{AR}=V_{AVDD}	-4.2	0.9	5.2	mV

Table 18. Low-power Comparator Input Threshold Using Internal Voltage Reference

Parameter	Condition	Min	Typ	Max	Unit
Low-power comparator threshold using internal reference voltage and low frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	0.90	0.96	1.04	V
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	0.89	0.96	1.04	V
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	0.89	0.96	1.05	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=1 kHz, V_{AR}=0V	1.02	1.03	1.05	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2V, T=85°C, f_{IN}=1 kHz, V_{AR}=0V	0.90	0.92	0.93	V
Low-power comparator threshold using internal reference voltage and median frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, f_{IN}=35 kHz, V_{REF}≈0.95V	0.89	0.95	1.04	V
	2.25V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, f_{IN}=35 kHz, V_{REF}≈0.95 V	0.89	0.96	1.04	V
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, f_{IN}=35 kHz, V_{REF}≈0.95 V	0.89	0.96	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62V, V_{DVDD}=1.2V, T=-40°C, f_{IN}=35kHz, V_{REF}≈0.95V	1.02	1.03	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=35kHz, V_{REF}≈0.95 V	0.90	0.91	0.93	V

Parameter	Condition	Min	Typ	Max	Unit
Low-power comparator threshold using internal reference voltage and high frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{REF}≈0.95 V	0.88	0.95	1.04	V
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{REF}≈0.95 V	0.89	0.95	1.04	V
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=70 kHz, V_{REF}≈0.95 V	0.88	0.95	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=70 kHz, V_{REF}≈0.95 V	1.01	1.03	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=70 kHz, V_{REF}≈0.95 V	0.89	0.91	0.92	V

Table 19. High-speed Comparator Input Threshold Using Internal Voltage Reference

Parameter	Condition	Min	Typ	Max	Unit
High-speed comparator threshold using internal reference voltage and low frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	0.90	0.96	1.04	V
High-speed comparator threshold using internal reference voltage and low frequency (Cont.)	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=1 kHz, V_{AR}=0V	0.90	0.96	1.04	V
	1.62V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98V, 1.62V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, f_{IN}=1kHz, V_{AR}=0V	0.90	0.96	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62V, V_{DVDD}=1.2V, T=-40°C, f_{IN}=1kHz, V_{AR}=0V	1.03	1.04	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=1kHz, V_{AR}=0V	0.90	0.92	0.93	V
High-speed comparator threshold using internal reference voltage and median frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, f_{IN}=300 kHz, V_{REF}≈0.95 V	0.90	0.96	1.04	V
	2.25V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=300 kHz, V_{REF}≈0.95 V	0.89	0.96	1.04	V
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, f_{IN}=300 kHz, V_{REF}≈0.95 V	0.89	0.96	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=300 kHz, V_{REF}≈0.95 V	1.03	1.03	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=300 kHz, V_{REF}≈0.95 V	0.90	0.92	0.93	V
High-speed comparator threshold using internal reference voltage and high frequency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{REF}≈0.95 V	0.90	0.96	1.04	V
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{REF}≈0.95 V	0.89	0.96	1.04	V
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{IN}=600 kHz, V_{REF}≈0.95 V	0.89	0.96	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{IN}=600 kHz, V_{REF}≈0.95 V	1.02	1.03	1.04	V
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{IN}=600 kHz, V_{REF}≈0.95 V	0.90	0.91	0.93	V

Table 20. Voltage Regulator (VR) Line Regulation

Parameter	Condition	Min	Typ	Max	Unit
Buck VR line regulation with ΔV_{PVDD}=±10%	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	6.7	12.4	mV/V
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	0.7	2.1	mV/V
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	500	1000	mV/V

Table 21. Voltage regulator (VR) Load Regulation

Parameter	Condition	Min	Typ	Max	Unit
Buck VR load regulation	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, ΔI_{DVDD}=50 mA	–	0.3	0.6	mV/mA
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, ΔI_{DVDD}=50 mA	–	0.3	1.5	mV/mA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, ΔI_{DVDD}=50 mA	–	5.1	8.5	mV/mA
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, ΔI_{DVDD}=5 mA	–	2.1	13.9	mV/mA

Table 22. Voltage Regulator (VR) Efficiency

Parameter	Condition	Min	Typ	Max	Unit
Buck VR efficiency	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, I_{DVDD}=50 mA	88.2	91.6	–	%
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, I_{DVDD}=50 mA	88.1	90.6	–	%
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, I_{DVDD}=50 mA	83.7	89.7	–	%
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, I_{DVDD}=5 mA	90.6	91.4	–	%

Table 23. I/O Pull-up Resistance

Parameter	Condition	Min	Typ	Max	Unit
I/O Pull-up resistance w/large voltage drop	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}<10 mV	33	39	54	kΩ
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, V_{IN}<10 mV	44	55	84	kΩ

Parameter	Condition	Min	Typ	Max	Unit
I/O Pull-up resistance w/large voltage drop (Cont.)	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}<10 mV	69	98	165	kΩ
	V_{PVDD}=V_{AVD}D=V_{IOVDD}=1.62 V, V_{DVDD}=1.2V, T=-40°C, V_{IN}<10 mV	130	136	141	kΩ
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, VIN<10 mV	35	35	36	kΩ
I/O Pull-up resistance w/large voltage drop	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}>V_{IOVDD}-10 mV	12	12	15	kΩ
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, V_{IN}>V_{IOVDD}-10 mV	15	16	20	kΩ
I/O Pull-up resistance w/large voltage drop (Cont.)	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}>V_{IOVDD}-10 mV	20	23	32	kΩ
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, V_{IN}>V_{IOVDD}-10 mV	24	25	26	kΩ
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, V_{IN}>V_{IOVDD}-10 mV	12	13	16	kΩ

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6.0 Timing Characteristics

Table 24. Time to Wake-Up From Comparator

Parameter	Condition	Min	Typ	Max	Unit
Wake-up time from standby on rising logic level using low-power comparator	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C	–	2.7	3.3	µs
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C	–	2.7	3.2	µs
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C	–	2.8	3.0	µs
Wake-up time from standby on rising logic level using high-speed comparator	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C	–	2.0	2.7	µs
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C	–	2.0	2.5	µs
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C	–	2.1	2.5	µs
Wake-up time from standby on falling logic level using low-power comparator	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C	–	5.3	7.1	µs
	2.25V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C	–	4.9	7.0	µs
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C	–	4.3	6.2	µs
Wake-up time from standby on falling logic level using high-speed comparator	3.00V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63V, -40≤T≤85°C	–	2.3	2.4	µs
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, -40≤T≤85°C	–	2.5	2.7	µs
	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.18 V, -40≤T≤85°C	–	2.5	2.7	µs
Wake-up time from retention on any logic transition using any comparator	1.82 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, -40≤T≤85°C	–	790	820	µs

Table 25. Comparator Bandwidth

Parameter	Condition	Min	Typ	Max	Unit
Low-power comparator bandwidth	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	77	111	127	kHz
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	93	128	137	kHz

Parameter	Condition	Min	Typ	Max	Unit
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	106	132	177	kHz
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2V, T=-40°C, V_{IN}=40 mV_{PP}	88	129	200	kHz
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, V_{IN}=40 mV_{PP}	115	125	133	kHz
High-speed comparator bandwidth	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	1.25	1.42	1.67	MHz
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	1.33	1.65	1.74	MHz
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	1.48	1.77	1.85	MHz
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, V_{IN}=40 mV_{PP}	1.37	1.54	1.67	MHz
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2V, T=85°C, V_{IN}=40 mV_{PP}	1.51	1.57	1.63	MHz

Table 26. Comparator Propagation Delay

PaVrameter	Condition	Min	Typ	Max	Unit
Low-power comparator propagation delay	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	–	2.28	4.65	µs
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	–	1.47	4.33	µs
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	–	1.33	3.77	µs
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, V_{IN}=40 mV_{PP}	–	1.54	1.67	µs
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, V_{IN}=40 mV_{PP}	–	1.83	2.50	µs
High-speed comparator propagation delay	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	–	134	319	ns
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	–	174	271	ns
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, V_{IN}=40 mV_{PP}	–	154	237	ns
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, V_{IN}=40 mV_{PP}	–	129	200	ns
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, V_{IN}=40 mV_{PP}	–	200	245	ns

Table 27. 33 MHz Crystal Oscillator Frequency Deviation

Parameter	Condition	Min	Typ	Max	Unit
33 MHz crystal oscillator frequency deviation using ABM8G-33.000 MHZ-4Y-T3 ±30 PPM crystal.	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C, f_{OSC}=33 MHz	56	58	59	PPM
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=33 MHz	55	57	59	PPM
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=33 MHz	55	58	77	PPM

Table 28. 32 kHz Crystal Oscillator Frequency Deviation

Parameter	Condition	Min	Typ	Max	Unit
32 kHz crystal oscillator frequency deviation using ABS06-32.768 KHZ-T ±20 PPM crystal.	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=32 kHz	31	61	61	PPM
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=32 kHz	57	61	61	PPM
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C, f_{OSC}=32 kHz	60	61	61	PPM
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=1.62 V, V_{DVDD}=1.2 V, T=-40°C, f_{OSC}=32 kHz	61	61	61	PPM
	V_{PVDD}=V_{AVDD}=V_{IOVDD}=3.63 V, V_{DVDD}=1.2 V, T=85°C, f_{OSC}=32 kHz	61	61	61	PPM

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7.0 ADC Performance Characteristics

All ADC performance characteristics were measured using the frequency domain techniques described in IEEE std. 1241.

Table 29. Offset After Calibration

Parameter	Condition	Min	Typ	Max	Unit
Offset at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	2.8	3.6	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	2.5	4.2	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	2.9	4.7	mV
Offset at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	5.6	7.2	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	5.2	7.9	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	4.4	7.2	mV
Offset at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	10.7	14.7	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	8.2	12.2	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	6.9	13.7	mV
Offset at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	29.3	35.4	mV
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	25.2	29.0	mV
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	20.0	24.9	mV

Table 30. Gain (Ideal Gain is Unity)

Parameter	Condition	Min	Typ	Max	Unit
Gain at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0051	1.0092	1.0163	–
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0036	1.0055	1.0177	–

Parameter	Condition	Min	Typ	Max	Unit
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0001	1.0050	1.0101	–
Gain at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0009	1.0104	1.0152	–
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0043	1.0056	1.0193	–
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0020	1.0085	1.0137	–
Gain at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0053	1.0073	1.0138	–
Gain at 8-bit resolution (Cont.)	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0020	1.0049	1.0122	–
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0029	1.0068	1.0138	–
Gain at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0010	1.0065	1.0146	–
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0010	1.0053	1.0116	–
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	1.0012	1.0065	1.0101	–

Table 31. Signal to Noise Ratio (SNR)

Parameter	Condition	Min	Typ	Max	Unit
SNR at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	67.1	69.1	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	66.4	68.1	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	65.5	67.7	–	dB
SNR at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	60.9	61.2	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	60.5	61.1	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	60.8	61.2	–	dB
SNR at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	49.2	49.4	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	49.3	49.5	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	49.5	49.7	–	dB
SNR at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	37.1	37.5	–	dB

Parameter	Condition	Min	Typ	Max	Unit
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	37.1	37.2	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	37.2	37.5	–	dB

Table 32. Total Harmonic Distortion (THD)

Parameter	Condition	Min	Typ	Max	Unit
THD at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-69.1	-68.3	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-69.8	-68.2	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-70.3	-65.7	dB
THD at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-69.6	-68.3	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-70.9	-68.3	dB
THD at 10-bit resolution (Cont.)	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-71.3	-63.1	dB
THD at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-70.0	-66.6	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-68.3	-64.5	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-69.2	-63.3	dB
THD at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-56.7	-53.4	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-61.6	-50.9	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	–	-56.0	-52.3	dB

Table 33. Spurious Free Dynamic Range (SFDR)

Parameter	Condition	Min	Typ	Max	Unit
SFDR at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	70.0	70.9	–	dB

Parameter	Condition	Min	Typ	Max	Unit
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	69.2	71.5	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	67.3	71.4	–	dB
SFDR at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	69.2	71.8	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	70.5	72.8	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	65.2	73.2	–	dB
SFDR at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	67.4	68.9	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	67.8	69.1	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	65.7	68.3	–	dB
SFDR at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	50.2	52.5	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	51.2	52.3	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	51.2	52.2	–	dB

Table 34. Signal to Interference, Noise and Distortion Ratio (SINAD)

Parameter	Condition	Min	Typ	Max	Unit
SINAD at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	64.9	66.2	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	63.0	65.5	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	62.8	65.9	–	dB
SINAD at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	60.2	60.6	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	59.5	60.5	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	58.8	60.8	–	dB
SINAD at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	49.1	49.4	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	49.3	49.4	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	49.5	49.6	–	dB
SINAD at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	37.1	37.4	–	dB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	37.0	37.2	–	dB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	37.2	37.4	–	dB

Table 35. Effective Number of Bits (ENOB)

Parameter	Condition	Min	Typ	Max	Unit
ENOB at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	10.5	10.7	–	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	10.4	10.7	–	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	10.1	10.7	–	LSB
ENOB at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	9.7	9.8	–	LSB

Parameter	Condition	Min	Typ	Max	Unit
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	9.7	9.8	–	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	9.5	9.8	–	LSB
ENOB at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	7.9	7.9	–	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	7.9	7.9	–	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	7.9	8.0	–	LSB
ENOB at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	5.9	5.9	–	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	5.9	5.9	–	LSB
ENOB at 6-bit resolution (Cont.)	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	5.9	5.9	–	LSB

Table 36. Differential Non-linearity (DNL)

Parameter	Condition	Min	Typ	Max	Unit
DNL at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C	-0.96	–	1.38	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.92	–	1.09	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.92	–	1.50	LSB
DNL at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.30	–	0.42	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.30	–	0.29	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.42	–	0.54	LSB
DNL at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.06	–	0.08	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98V, -40≤T≤85°C	-0.08	–	0.09	LSB

Parameter	Condition	Min	Typ	Max	Unit
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.14	–	0.20	LSB
DNL at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.03	–	0.07	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.05	–	0.12	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.01	–	0.06	LSB

Table 37. Integral Non-linearity (INL)

Parameter	Condition	Min	Typ	Max	Unit
INL at 12-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-1.77	–	1.90	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-1.69	–	1.85	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-1.59	–	2.48	LSB
INL at 10-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.61	–	0.42	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.60	–	0.44	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.61	–	0.81	LSB
INL at 8-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.11	–	0.10	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.14	–	0.11	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.15	–	0.20	LSB
INL at 6-bit resolution	3.00 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤3.63 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.04	–	0.06	LSB
	2.25 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤2.75 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.06	–	0.06	LSB
	1.62 V≤V_{PVDD}=V_{AVDD}=V_{IOVDD}≤1.98 V, 1.62 V≤V_{DVDD} ≤1.98 V, -40≤T≤85°C	-0.06	–	0.06	LSB

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8.0 Package Outline

Figure 15. Package Outline Bottom and Side Views

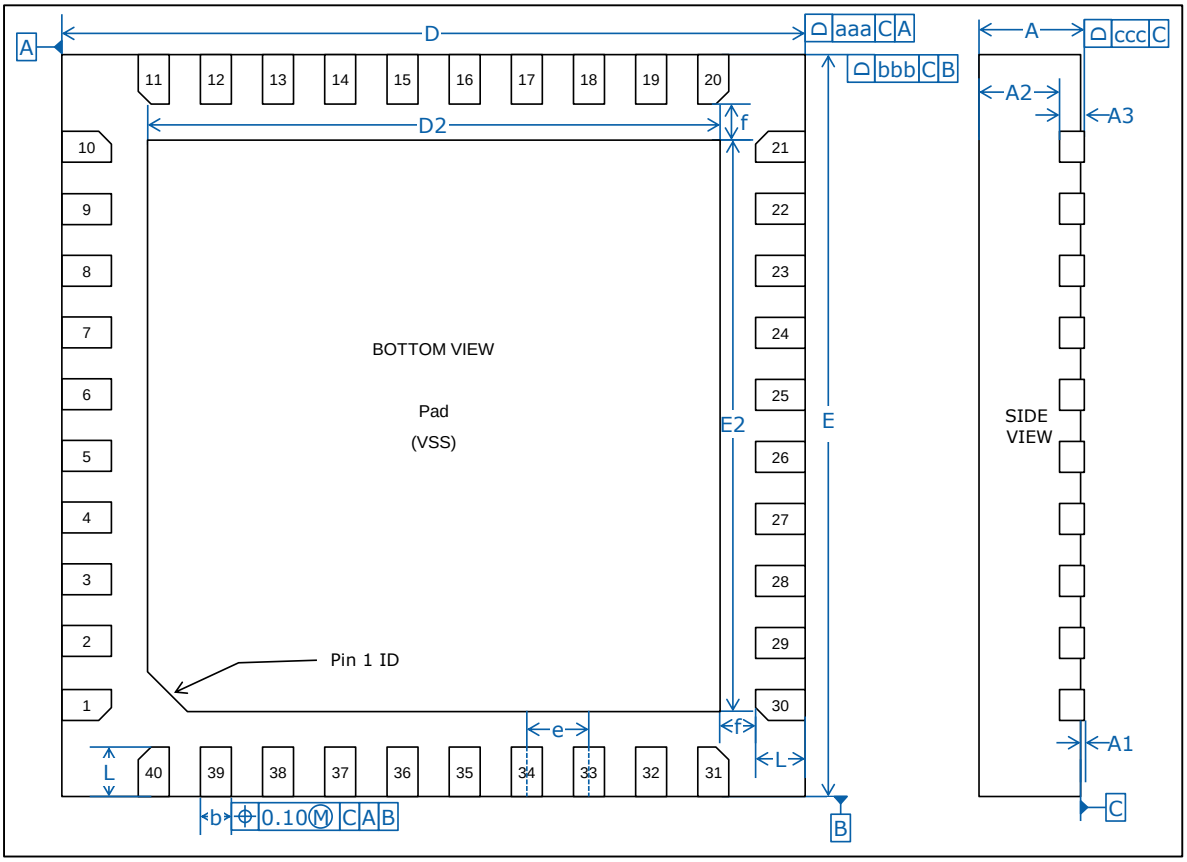
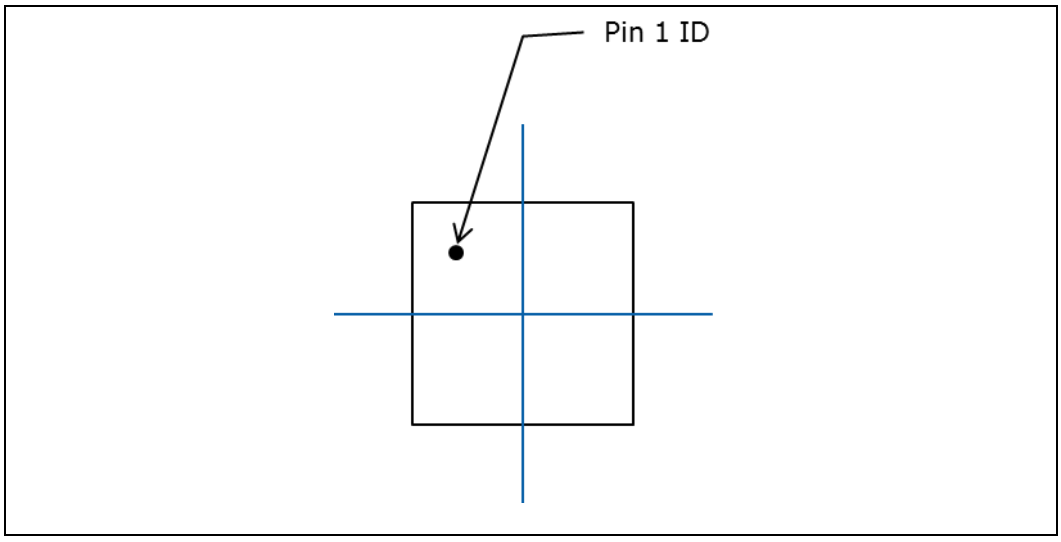


Table 38. Dimensions in mm

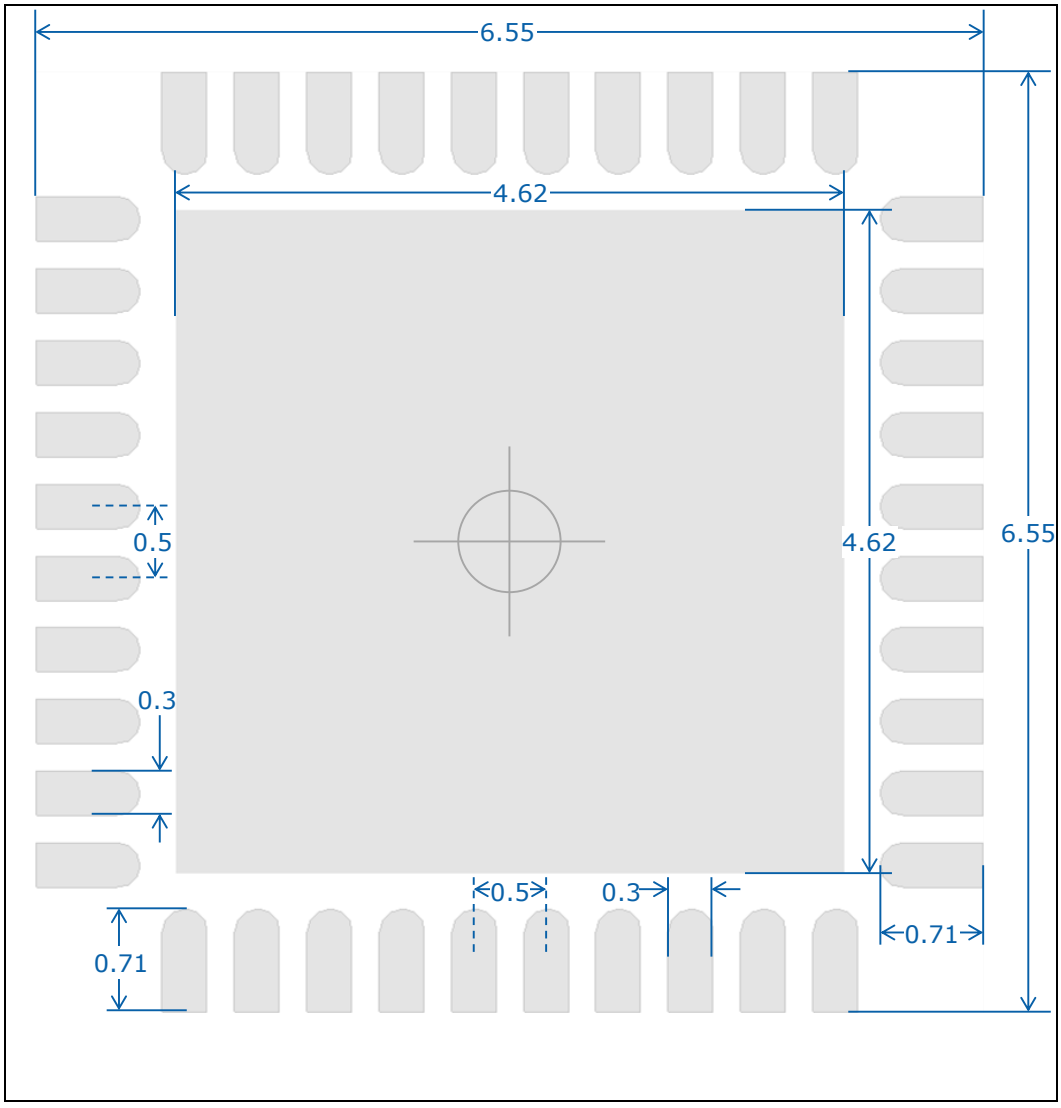
Symbol	Minimum	Nominal	Maximum
A	0.75	0.85	0.90
A1	0.00	0.035	0.05
A2	---	0.65	0.67
A3	0.203 REF.		
b	0.20	0.25	0.30
D	5.90	6.00	6.10
D2	4.52	4.62	4.72
E	5.90	6.00	6.10
E2	4.52	4.62	4.72
e	0.50 bsc		
f	0.20	---	---
L	0.35	0.40	0.45
Tolerances of Form and Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		

Figure 16. Pin 1 ID (Top View)



9.0 Suggested Footprint

Figure 17. 40 QFN Package Land Pattern Dimensions (in mm)



Note: Customers should check with their board fabrication house for minimum solder mask web tolerances between signal pads.

Note: Stencils should be laser cut, with trapezoidal walls and rounded corners for better paste release. Generally speaking, the stencil for the center pad should be an array of smaller openings covering 50-85% of the pad area. Customers should check with their board assembly house for solder stencil design recommendations.

10.0 References

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- ARM Limited. (2004). AMBA 3 APB Protocol Specification. Cambridge, UK: ARM.
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